

KA3525A

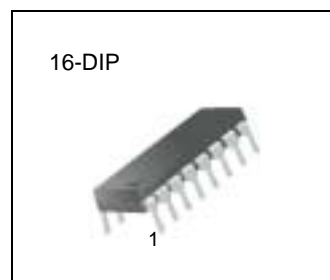
SMPS Controller

Features

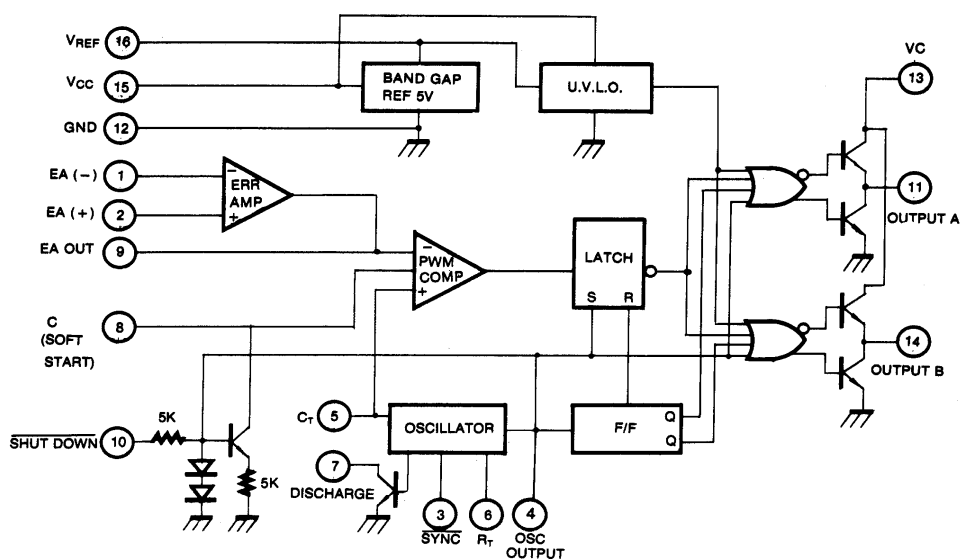
- 5V ± 1% Reference
- Oscillator Sync terminal
- Internal Soft Start
- Deadtime Control
- Under-Voltage Lockout

Description

The KA3525A is a monolithic integrated circuit that includes all of the control circuit necessary for a pulse width modulating regulator. There are a voltage reference, an error amplifier, a pulse width modulator, an oscillator, under-voltage lockout, soft start circuit, and output drivers in the chip.



Internal Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	40	V
Collector Supply Voltage	V _C	40	V
Output Current, Sink or Source	I _O	500	mA
Reference Output Current	I _{REF}	50	mA
Oscillator Charging Current	I _{CHG(OSC)}	5	mA
Power Dissipation (T _A = 25°C)	P _D	1000	m/W
Operating Temperature	T _{OPR}	0 ~ +70	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C
Lead Temperature (Soldering, 10 sec)	T _{LEAD}	+300	°C

Electrical Characteristics

(V_{CC} = 20V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
Reference Output Voltage	V _{REF}	T _J = 25°C	5.0	5.1	5.2	V
Line Regulation	ΔV _{REF}	V _{CC} = 8 to 35V	-	9	20	mV
Load Regulation	ΔV _{REF}	I _{REF} = 0 to 20mA	-	20	50	mV
Short Circuit Output Current	I _{SC}	V _{REF} = 0, T _J = 25°C	-	80	100	mA
Total Output Variation (Note 1)	ΔV _{REF}	Line, Load and Temperature	4.95	-	5.25	V
Temperature Stability (Note 1)	ST _T	-	-	20	50	mV
Long Term Stability (Note 1)	ST	T _J = 125°C, 1 KHRs	-	20	50	mV
OSCILLATOR SECTION						
Initial Accuracy (Note 1, 2)	ACCUR	T _J = 25°C	-	± 3	± 6	%
Frequency Change With Voltage	Δf/ΔV _{CC}	V _{CC} = 8 to 35V (Note 1, 2)	-	± 0.8	± 2	%
Maximum Frequency	f _(MAX)	R _T = 2KΩ, C _T = 470pF	400	430	-	KHz
Minimum Frequency	f _(MIN)	R _T = 200KΩ, C _T = 0.1uF	-	60	120	Hz
Clock Amplitude (Note 1, 2)	V _(CLK)	-	3	4	-	V
Clock Width (Note 1, 2)	t _{W(CLK)}	T _J = 25°C	0.3	0.6	1	μs
Sync Threshold	V _{TH(SYNC)}	-	1.2	2	2.8	V
Sync Input Current	I _{I(SYNC)}	Sync = 3.5V	-	1.3	2.5	mA

Electrical Characteristics

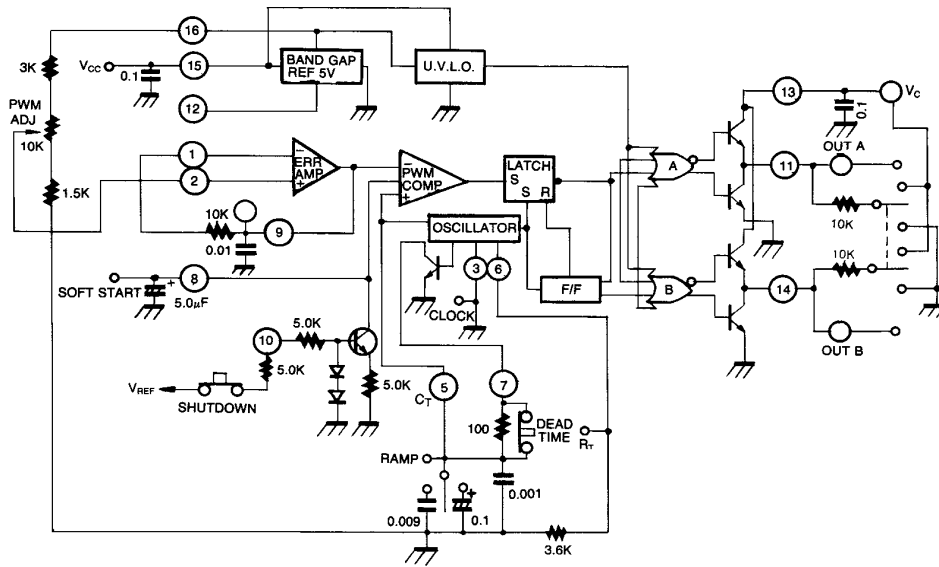
($V_{CC} = 20V$, $T_A = 0$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1V$)						
Input Offset Voltage	V_{IO}	-	-	1.5	10	mV
Input Bias Current	I_{BIAS}	-	-	1	10	μA
Input Offset Current	I_{IO}	-	-	0.1	1	μA
Open Loop Voltage Gain	G_{VO}	$R_L \geq 10M\Omega$	60	80	-	dB
Common Mode Rejection Ratio	CMRR	$V_{CM} = 1.5$ to $5.2V$	60	90	-	dB
Power Supply Rejection Ratio	PSRR	$V_{CC} = 8$ to $3.5V$	50	60	-	dB
PWM COMPARATOR SECTION						
Minimum Duty Cycle	$D(MIN)$	-	-	-	0	%
Maximum Duty Cycle	$D(MAX)$	-	45	49	-	%
Input Threshold Voltage (Note 2)	V_{TH1}	Zero Duty Cycle	0.7	0.9	-	V
Input Threshold Voltage (Note 2)	V_{TH2}	Max Duty Cycle	-	3.2	3.6	V
SOFT-START SECTION						
Soft Start Current	I_{SOFT}	$V_{SD} = 0V$, $V_{SS} = 0V$	25	51	80	μA
Soft Start Low Level Voltage	V_{SL}	$V_{SD} = 25V$	-	0.3	0.7	V
Shutdown Threshold Voltage	$V_{TH(SD)}$	-	0.6	0.8	1	V
Shutdown Input Current	$I_{N(SD)}$	$V_{SD} = 2.5V$	-	0.3	1	mA
OUTPUT SECTION						
Low Output Voltage I	$V_{OL I}$	$I_{SINK} = 20mA$	-	0.1	0.4	V
Low Output Voltage II	$V_{OL II}$	$I_{SINK} = 100mA$	-	0.05	2	V
High Output Voltage I	$V_{CH I}$	$I_{SOURCE} = 20mA$	18	19	-	V
High Output Voltage II	$V_{CH II}$	$I_{SOURCE} = 100mA$	17	18	-	V
Under Voltage Lockout	V_{UV}	V_8 and $V_9 = High$	6	7	8	V
Collector Leakage Current	I_{LKG}	$V_{CC} = 35V$	-	80	200	μA
Rise Time (Note 1)	t_R	$C_L = 1\mu F$, $T_J = 25^{\circ}C$	-	80	600	ns
Fall Time (Note 1)	t_F	$C_L = 1\mu F$, $T_J = 25^{\circ}C$	-	70	300	ns
STANDBY CURRENT						
Supply Current	I_{CC}	$V_{CC} = 35V$	-	12	20	mA

Notes :

1. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production
2. Tested at $f_{OSC} = 40$ KHz ($R_T = 3.6K$, $C_T = 0.01\mu F$, $R_I = 0\Omega$)

Test Circuit



Mechanical Dimensions

Package

16-DIP

