1. Description

(1) Large capacity graphics type capable of displaying numerics, alphabetics, special characters, graphs, charts, and patterns

(2) 4 bits parallel chip enable method for data transference

(3) FTN (Formulated STN) - FEM Technology

(4) Negative display

(5) Transmissive type

(6) 1/242 duty multiprexing drive V - 13.1 V

(Do not use this module by 1/240 and/or 1/241 duty)

(7) Colors

Display dots ---- White

Background ---- Black

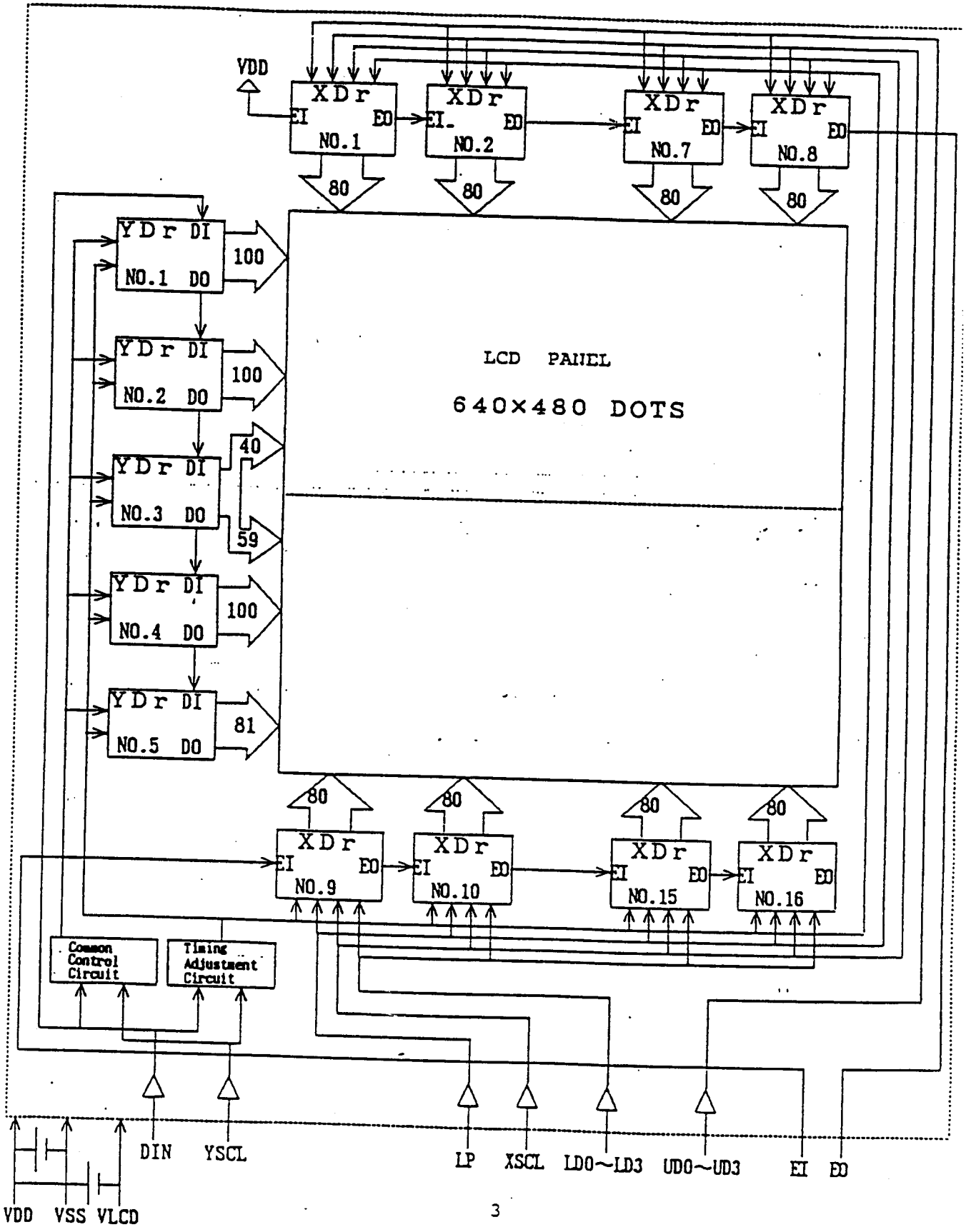
(8) Backlight : Cold Cathod Fluorescent Lamp

2. Mechianical Specifications

Item	Specifications
Dot matrix	640 x 480 (dots)
Overall dimensions (W x H x D)	253.5 x 160.0 x 15.0 (MAX)
Viewing area (W x H)	180.0 x 134.6
Active area (L x W)	172.765 x 129.565
Dot pitch (L x W)	0.27 x 0.27
Dot size (L x W)	0.235 x 0.235

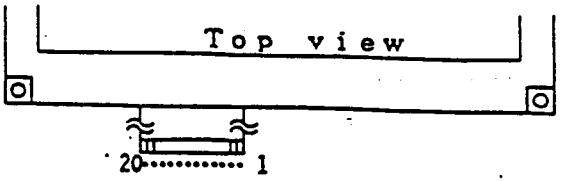
Unit : mm

3. Block diagram



4. I/O Terminals

4.1 Terminal Configuration



4.2 Terminal Functions

Pin No.	Signal	Name	Function
1	VDD	Power Supply Voltage	+5.0V±5%
2	VSS	GND	0V
3	VLCD	Power Supply (LCD)	Contrast Variable Power
4	LP	Latch Pulse	Data Latch
5	NC	NC	---
6	NC	NC	---
7	YSCL	Y Shift Clock	Data Shift Clock
8	DIN	Synchronous Pulse	Scan Start Pulse
9	XSCL	X Shift Clock	Data Shift Clock
10	NC	NC	---
11	UD0	Data	Display Data Input for Upper Half Screen
12	UD1		
13	UD2		
14	UD3		
15	LD0	Data	Display Data Input for Lower Half Screen
16	LD1		
17	LD2		
18	LD3		
19	EI	Enable IN	Enable Signal Input for XDr(5) *
20	EO	Enable OUT	Connecting with VSS Internally

LP

+5V

N.C.

* 4 bit input : Connect EI EI to EO
  8 bit input : EI - VDD, EO - NC

5. DATA INPUT FORMAT (640 x 480 dots)

5.1 Display Dot Map

Column→ / Row ↓	1 D	2 D	3 D	4 D	5 D	6 D	...	635 D	636 D	637 D	638 D	639 D	640 D
1 D	1 . 1	1 . 2	1 . 3	1 . 4	1 . 5	1 . 6		1 .635	1 .636	1 .637	1 .638	1 .639	1 .640
2 D	2 . 1	2 . 2	2 . 3	2 . 4	2 . 5	2 . 6		2 .635	2 .636	2 .637	2 .638	2 .639	2 .640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	⋮
239 D	239.1	239.2	239.3	239.4	239.5	239.6		239.635	239.636	239.637	239.638	239.639	239.640
240 D	240.1	240.2	240.3	240.4	240.5	240.6		240.635	240.636	240.637	240.638	240.639	240.640
241 D	1 . 1	1 . 2	1 . 3	1 . 4	1 . 5	1 . 6		1 .635	1 .636	1 .637	1 .638	1 .639	1 .640
242 D	2 . 1	2 . 2	2 . 3	2 . 4	2 . 5	2 . 6		2 .635	2 .636	2 .637	2 .638	2 .639	2 .640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	⋮
479 D	239.1	239.2	239.3	239.4	239.5	239.6		239.635	239.636	239.637	239.638	239.639	239.640
480 D	240.1	240.2	240.3	240.4	240.5	240.6		240.635	240.636	240.637	240.638	240.639	240.640

The previous display dot map shows the entry order of data in terms of dots on the LCD.
Display data is sequentially entered in each UD0~UD3, LD0~LD3 on a 4 bits basis, from left to right, beginning with location "1.1".
This display from 1.1 ~ 1.4, 1.5 ~ 1.8, ... to 1.640 on a 4 dots (bits) basis.

5.2 Correspondence of Data Input Terminals to Dot Numbers in a Row

Data Input Terminal	Dots (Row) on Display
UD0 / LD0	dot 4, dot 8 ..... dot 636, dot 640
UD1 / LD1	dot 3, dot 7 ..... dot 635, dot 639
UD2 / LD2	dot 2, dot 6 ..... dot 634, dot 638
UD3 / LD3	dot 1, dot 5 ..... dot 633, dot 637

Input data UD0~UD3, LD0~LD3 correspond to display dots as shown above. The first input data corresponds to dot 4~1, and the last input data to dot 640~637.

5.3 Data Input Method

This module uses "Chip Enable Transmission System" to reduce its power consumption. Data is inputted directly into LCD drivers (chips) on a chip basis. If the n-th chip in enable state becomes full of data, the Enable is transmitted by automaticaly to (n+1)th chip.

There are two methods to input signal into display as described below.

(1) To input the signal on 4 bit-bus with one line.(UD0~UD3)
In case of using the controller which outputs the signal on 4 bit-bus with one line, at first to short circuit the No.19 and 20th pin on I/O terminals and to connect UD0 and LD0, UD1 and LD1, UD2 and LD2, UD3 and LD3. Next, to input the signal from UD0 to UD3.
In this case signal shall be input from 1.1 ~ 1.640 {XDr(1) to XDr(8)} with each 4 bit into Upper screen, after that signal shall be input Lower screen by same system as Upper screen{XDr(9) to XDr(16)}.

(2) To input the signal on 4 bit-bus with two line (UD0~UD3,LD0~LD3)
In case of using the controller which outputs the signal on 4 bit-bus with two line, to connect No.19 pin with VDD level and to open No.20 pin on I/O terminals. Next, to input the signal from UD0,LD0 to UD3,LD3 in parallel.
In this case, signal shall be input from 1.1 ~ 1.640 with each 4 bit into Upper and Lower screen at the same time.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Standard value	Unit
Supply Voltage	VDD - VSS	0 ~ + 7.0	V
	VDD - VEE	0 ~ + 28.0	
Input Voltage	VIN	VSS ≧ VIN ≧ VDD	
Operating Temperature	Top	+ 5 ~ + 40	°C
Storage Temperature	Tst	- 20 ~ + 60	

7. ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

Ta=25°C
VDD=5V±5%.

Parameter	Symbol	Standard value			Unit	Applicable Terminal	Condition
		Min	Typ	Max			
Supply Voltage	VDD	4.75	5.0	5.25	V	VDD	
Supply voltage	VLCD	VDD-28	-	-	V	VLCD	
"0" input voltage	VIL	-	-	0.2VDD	V	UD0~UD3 LD0~LD3 XSCL,LP YSCL,DIN	
"1" input voltage	VIH	0.8VDD	-	-	V		
"0" input leakage current	IIL	50	-	-	μA		
"1" input leakage current	IIH	-	-	50	μA		
Supply current (Logic)	IDD	-	20.0	35.0	mA	VDD	VDD=5.0V VLCD=-17.4V fFR=70 Hz
Supply Current (LCD)	ILCD	-	10.0	25.0	mA	VLCD	

7.2 AC Characteristics

Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
FR delay time	TFD	- 500	0	500	nsec	VDD = 5V ± 5%
DIN period	TDIC	12	13.3	15	msec	
XSCL period	TXSC	166	-	-	nsec	
LP "L" time	TLL	330	-	-	nsec	
LP pulth width	WLP	70	-	-	nsec	
YSCL "L" time	TYSL	330	-	-	nsec	
YSCL pulth width	WYSL	70	-	-	nsec	
XSCL "L" time	TXSL	70	-	-	nsec	
XSCL pulth width	WXSC	70	-	-	nsec	
Latch timing	TLS1	70	-	-	nsec	
	TLS2	70	-	-		
	TLS3	70	-	-		
	TLD	0	-	-		
Data set up time	TDS	60	-	-	nsec	
Data hold time	TDH	40	-	-	nsec	
DIN set up time	TDIS	100	-	-	nsec	
DIN hold time	TDIH	10	-	-	nsec	
Rise & Fall time	tr,tf	-	-	*	nsec	

* ----- (TXSC - TXSL - WXSC)/2 with 50 ns Max.