富相科技股份有限公司
SOLOMON Goldentek Display Corp.

KAOHSIUNG FACTORY : NO. 18 Ta-Yeh St., Ta-Fa Industrial Park,Ta-Liao Hsiang, Kaohsiung Hsien 831, TAIWAN , R.O.C.
TEL : 886-7-788-6800
FAX : 886-7-788-6806~8

PART NO : GG1203N4SKY1B(LM6480SGL)
FOR MESSRS : _____

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Accepted by :_____ Proposed by :_____
Date : 09,11,2002

RECORD OF REVISION

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	06	OPTICAL CHARACTERISTICS. CONTRAST RATIO K=4 →2.5 RESPONSE TIME tr TYP. TBA → --- MAX . TBA →250 tf TYP .TBA → --- MAX. TBA→250 THE BRIGHTNESS OF BACKLIGHTING SOURCE SYMBOL ----→ B MIN.4.0 → ----- TYP .----→2.0
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3. GENERAL SPECIFICATIONS AND MECHANICAL DATA

3.1 GENERAL SPECIFICATIONS

PLEASE REFER TO :

”CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (SP-10-000)”.

3.2 THIS INDIVIDUAL SPECIFICATIONS IS PRIOR TO GENERAL SPECIFICATIONS.

3.3 MECHANICAL DATA

(1) NUMBER OF DOTS ---------- 128W× 32H DOTS

(2) MODULE SIZE ---------- 76.0W× 30.0H× 12.0T (MAX) mm

(3) VEWING AREA ---------- 63.0W× 17.5H mm

(4) DOT SIZE ---------- 0.45W× 0.45H mm

(5) DOT PITCH ---------- 0.48W× 0.48H mm

(6) VIEWING DIRECTION ---------- 6 O’CLOCK

(7) LED COLOR ---------- YELLOW-GREEN

(8) LCD COLOR ---------- STN , GRAY , TRANSFLECTIVE

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD-VSS	2.4	6.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY	———	——	100	V	NOTE(1)
POWER SUPPLY FOR LED	VLED-GND	——	6.0	V	

NOTE(1) : TEST METHOD AND CONDITIONS AFTER CHARGING UP 200PF CAPACITOR BY STATED VOLTAGE , THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RAINGS.

ITEM	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	0℃	50℃	-20℃	60℃	NOTE(2)
HUMIDITY	NOTE(3)		NOTE(3)		WITHOUT CONDENSATION
VIBRATION	——	4.9 m/s^2 (0.5G)	——	19.6 m/s^2 (2G)	
SHOCK	——	29.4 m/s^2 (3G)	——	49.0 m/s^2 (5G)	XYZ DIRECTIONS
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE(2) : Ta AT -20℃ : 48HR MAX.
Ta AT 60℃ : 168HR MAX.

NOTE(3) : Ta ≦ 40℃ : 90% RH MAX.
Ta ＞ 40℃ : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40℃. (50% RH AT 50℃)

5. ELECTRICAL AND CHARACTERISTICS

Ta = 25℃ VDD = 5.0V ± 0.25V

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-VSS	———	2.4	——	6.0	V
INPUT VOLTAGE	VIH	HI LEVEL	0.3*VSS	——	VDD	V
	VIO	LOW LEVEL	VSS	——	0.7*VSS	V
OUTPUT VOLTAGE	VOH	HI LEVEL	0.2*VDD	——	VDD	V
	VOL	LOW LEVEL	VSS	——	0.8*VSS	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	IDD	VDD-VSS =5.0V	——	0.3	1.0	mA
RECOMMENDED LCD DRIVING VOLTAGE (NOTE 2)	VDD - VO	Ta = 0℃	——	(6.6)	——	V
	DUTY = 1/32	Ta = 25℃	——	6.1	——	V
	∮ = 10°	Ta = 50℃	——	(5.6)	——	V
THE POWER SUPPLY FOR LED	ILED	V_{LED+}-V_{LED-}=5.0V	——	210	——	mA

NOTE(1) : CS1 , CS2 , R/W , A0 ,E, DB0~DB7

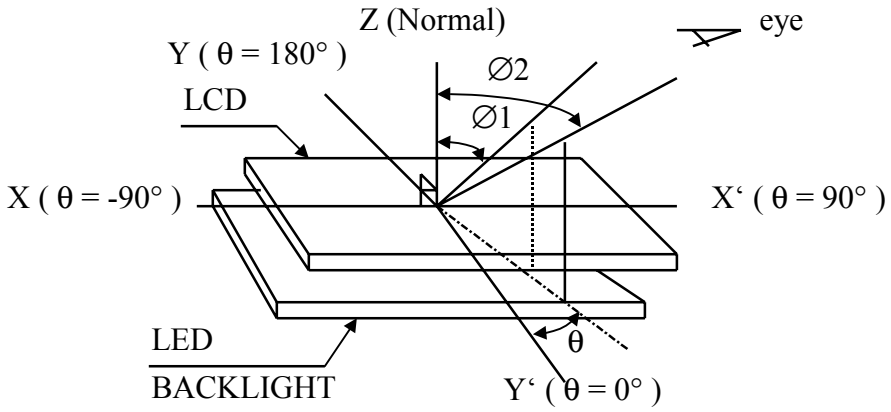
NOTE(2) : RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT ± 0.5V BY EACH MODULE.

6. OPTICAL CHARACTERISTICS.

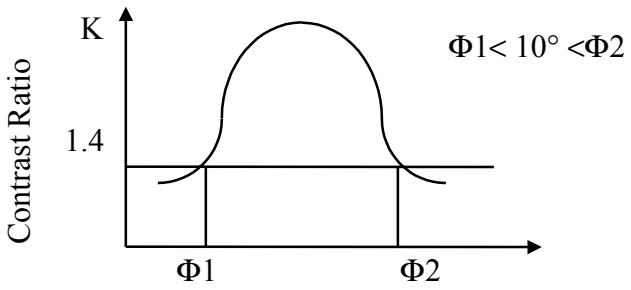
Ta = 25°C VDD = 5.0V ± 0.25V

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING AREA	Φ2-Φ1	K≧ 1.4	20	40	——	deg.	1
CONTRAST RATIO	K	Φ = 10° θ = 0°	——	1.5	——	——	2,3
RESPONSE TIME	tr(rise)	Φ = 10° θ = 0°	——	——	250	ms	4
	tf(fall)	Φ = 10° θ = 0°	——	——	250	ms	4
THE BRIGHTNESS OF BACKLIGHTING SOURCE(LCM)	B	Φ = 0° θ = 0°	——	20	——	cd/m^2	5
	λp	——	565	570	575	nm	

NOTE (1) : DEFINITION OF θ AND Φ



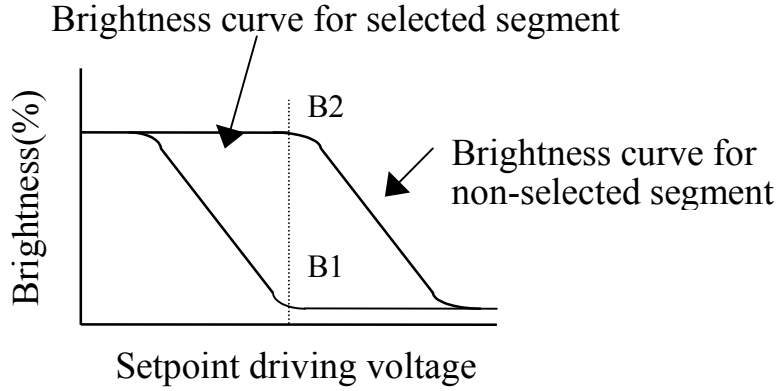
NOTE (2) : DEFINITION OF VIEWING ANGLE Φ1 AND Φ2



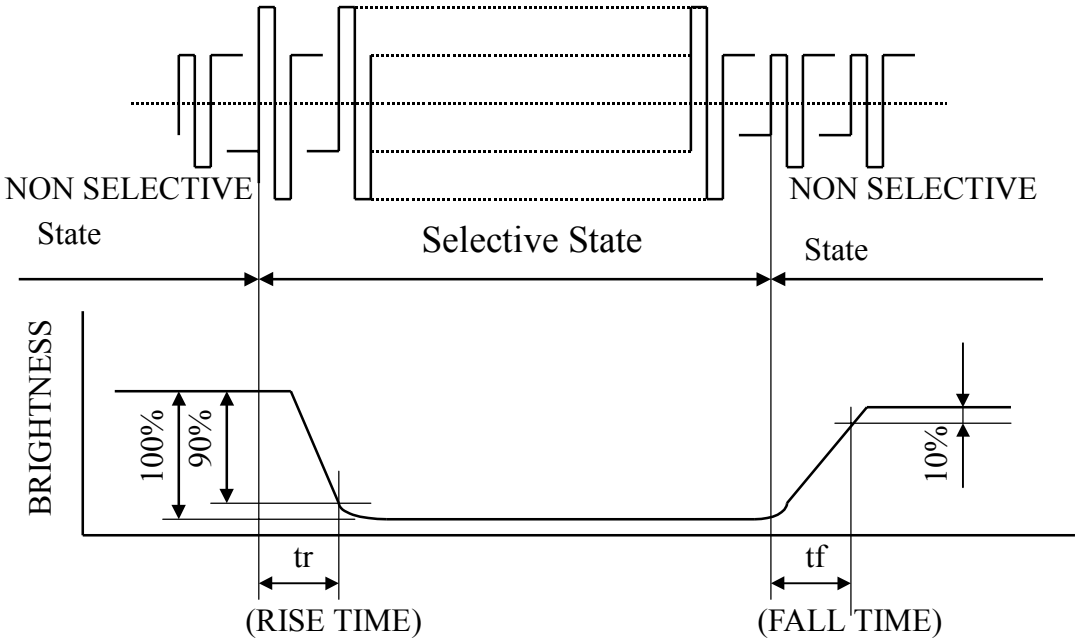
Viewing Angle

NOTE (3) : DEFINITION OF CONTRAST"K"

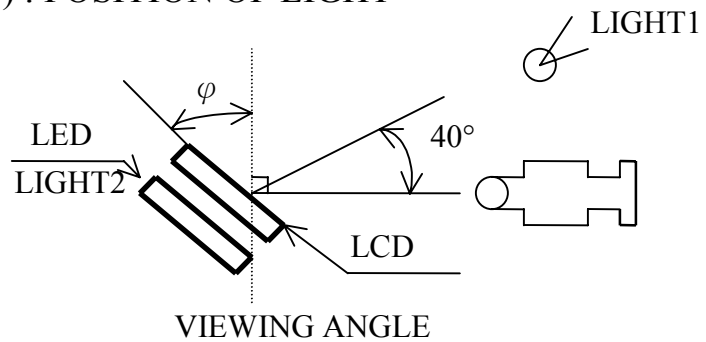
$$K = \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$



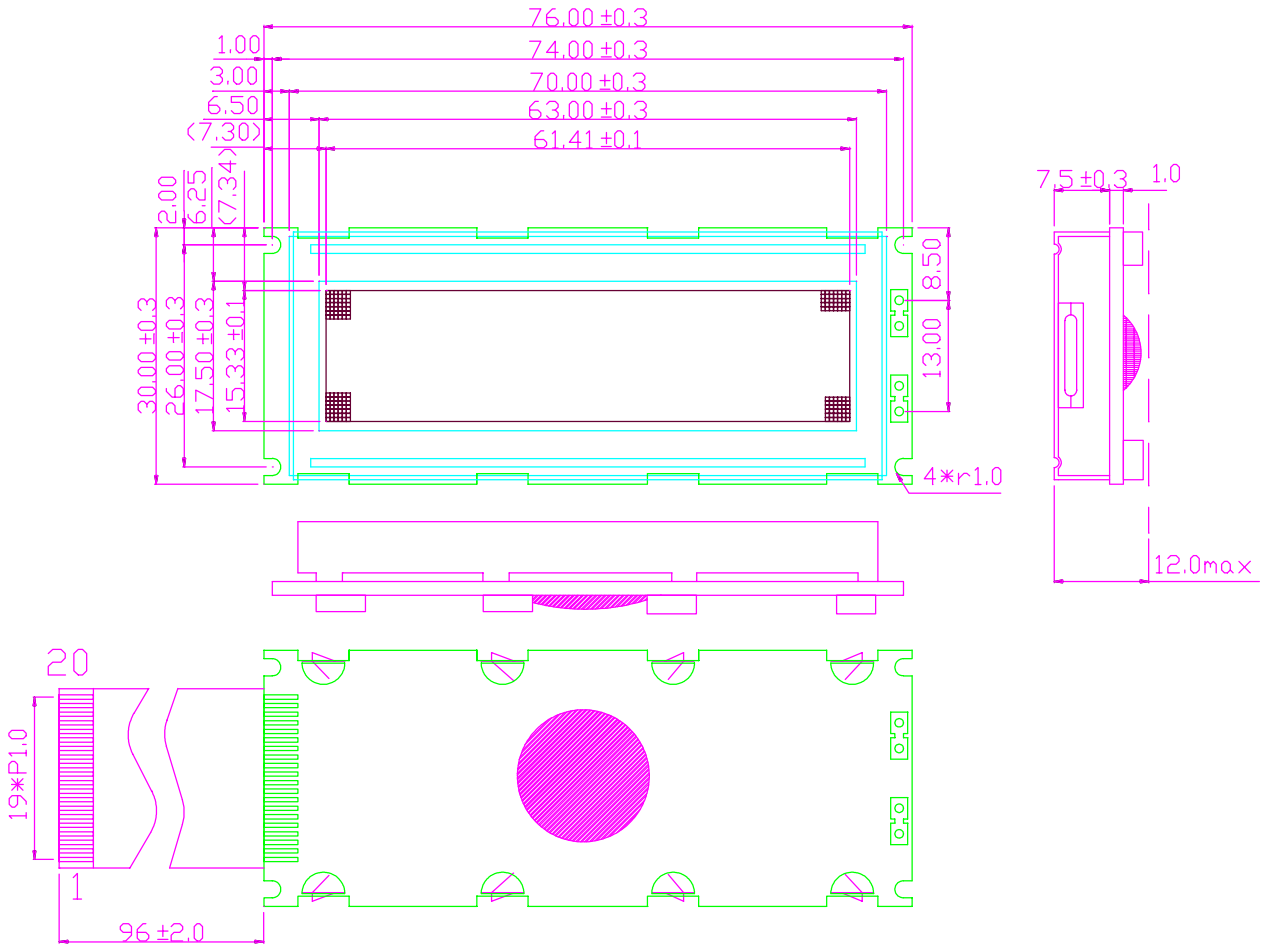
NOTE(4) : DEFINITION OF OPTICAL RESPONSE



NOTE (5) : POSITION OF LIGHT



6. OUTLINE DIMENSION

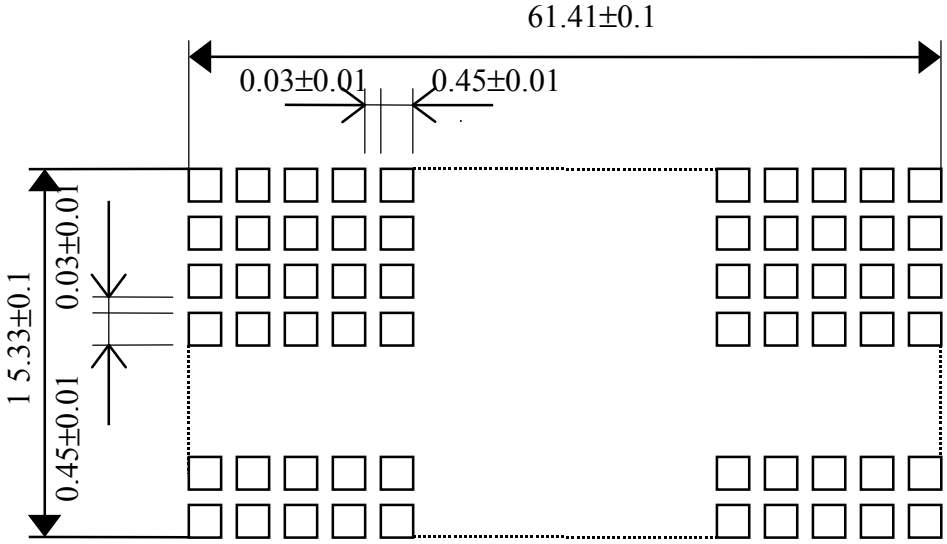


NUIT : mm
SCALE : NTS
NON-SPECIFIED TOLERANCE ±0.3

INTERFACE PIN CONNECTION:

NO.	1	2	3	4	5	6	7	8	9	10
SYMBOL	VSS	VDD	VO	Vout	A0	R/$\overline{W}$	E	DB0	DB1	DB2
NO.	11	12	13	14	15	16	17	18	19	20
SYMBOL	DB3	DB4	DB5	DB6	DB7	C86	$\overline{CS1}$	CS2	LED(+)	LED(-)

NOTE 1. DETAIL DRAWING OF MATRIX PATTERN

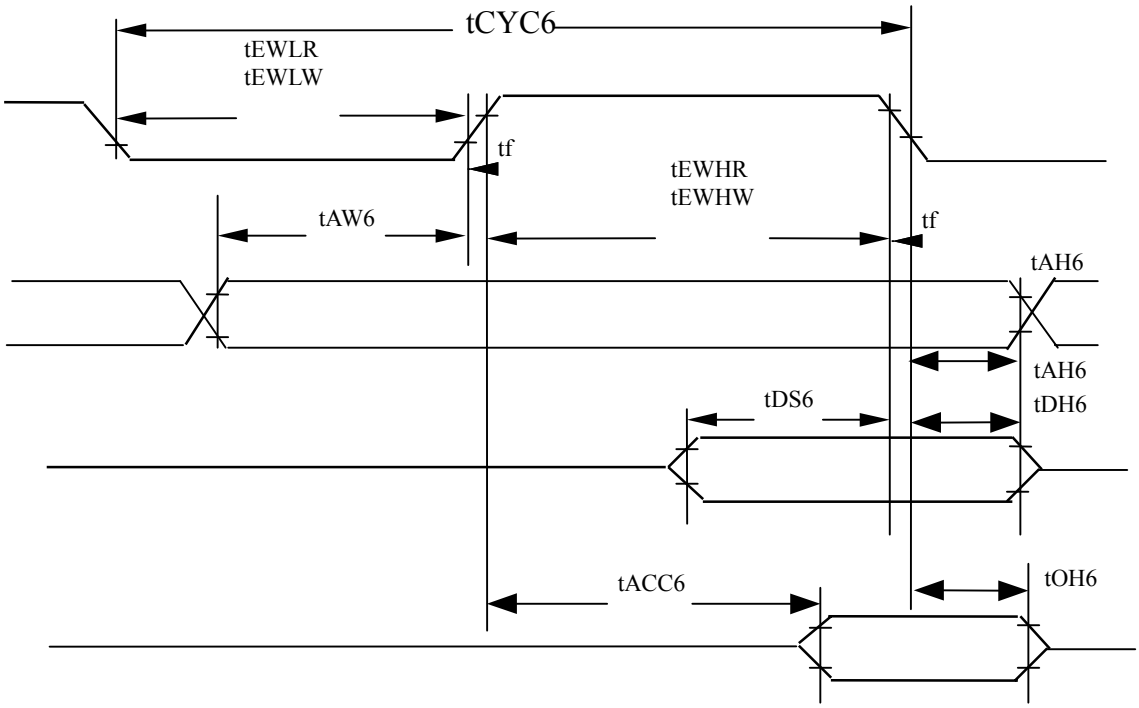


NOTE 2 . INTERNAL PIN CONNECTION

PIN NO	SYMBOL	LEVEL	FUNCTION
1	VSS	——	GROUND
2	VDD	——	POWER SUPPLY FOR LOGIC CIRCUIT
3	VO	——	OPERATING VOLTAGE FOR LCD DRIVING
4	Vout		POWER SUPPLY FOR LCD DRIVING (-9V)
5	A0	H/L	H : DATA INPUT L : INSTRUCTION CODE INPUT
6	R/$\overline{W}$	H/L	H : DATA READ (LCD MODULE → MPU) L : DATA WRITE (LCD MODULE ← MPU)
7	E	H,H→L	ENABLE SINGNAL
8 | 15	DB0 | DB7	H/L	DATA BUS LINE
16	C86	H/L	H : 6800 Series L : 8080 Series
17	/CS1	H	CHIP SELECTION FOR IC1
18	CS2	H	CHIP SELECTION FOR IC2
19	LED(+)	——	POWER SUPPLY FOR LED BACKLIGHT
20	LED(-)	——	POWER SUPPLY FOR LED BACKLIGHT

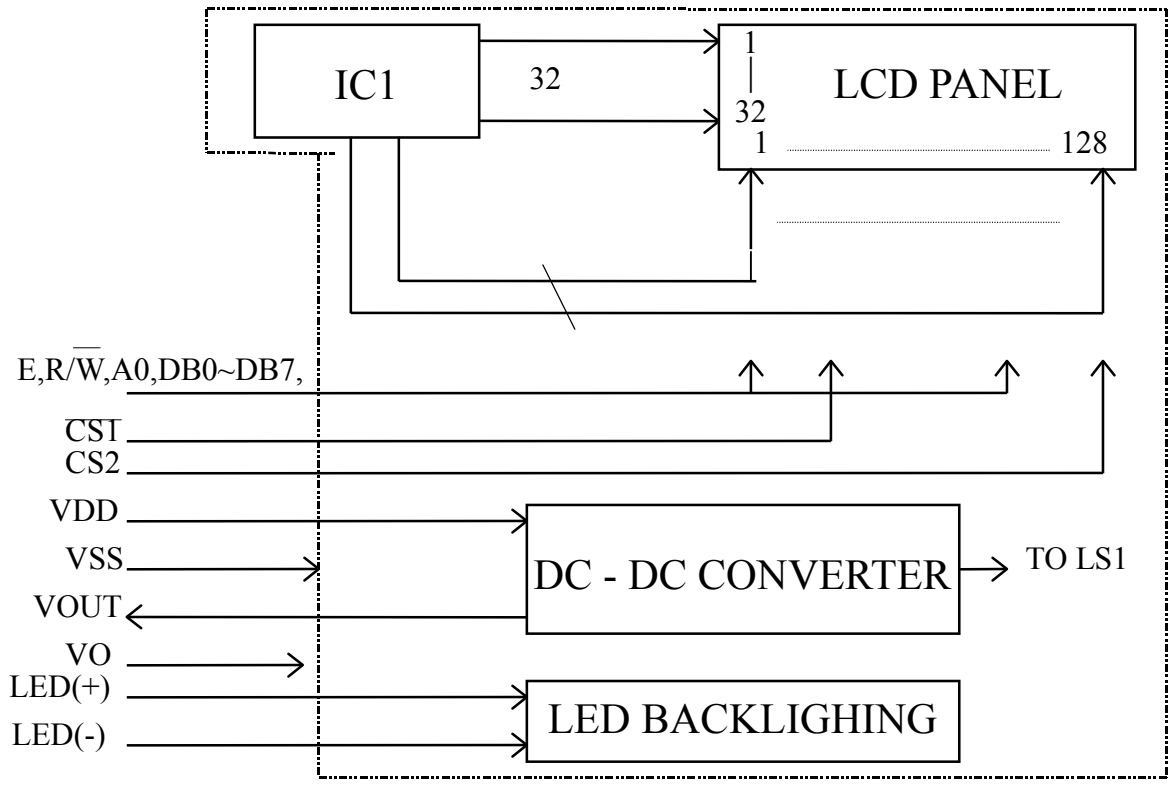
Vss=-5.0V± 10%,Ta=-30~85℃

Item		Sgnal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			tCYC6		200		ns
Address setup time address hold time		(A0) R/$\overline{W}$	tAW6 tAH6		10 10		ns ns
Data setup time Data hold time		D0-D7	tDS6 tDH6		20 10		ns ns
Output disable time Access time			tOH6 tACC5	CL=100Pf	10	50 70	ns ns
Enable H pulse width	READ	E	tEWHR tEWHW		77		ns
	WRITE				22		ns
Enable L pulse width	READ	E	tEWLR tEWLW		117		ns
	WRITE				172		ns
Input signal change time			tr,tf			15	ns

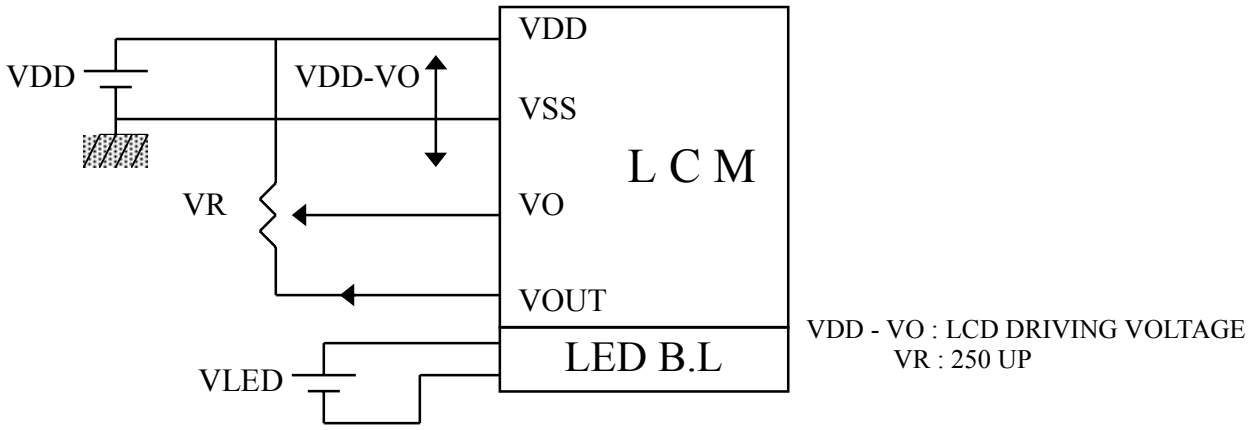


7. BLOCK DIAGRAM AND POWER SUPPLY

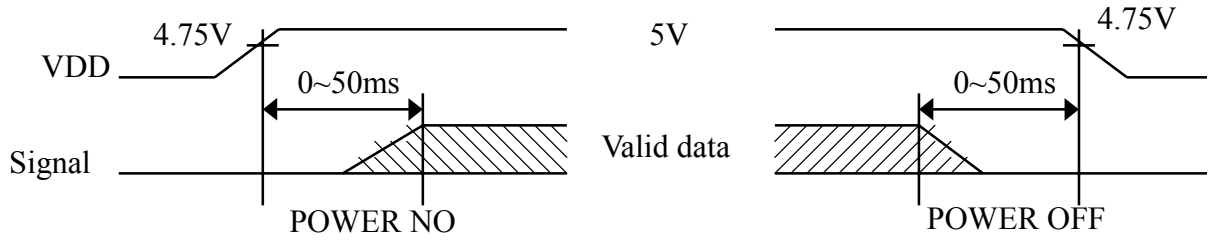
7.1 BLOCK DIAGRAM



7.2 POWER SUPPLY FOR LCM



7.3 POWER AND INTERFACE TIMING SEQUENCE



8. FUNCTION OF EACH BLOCK

Interface Control

Parallel interface

Parallel data can be transferred in either direction between the controlling microprocessor and the LCM through the 8-bit I/O D0 to D7).The type of microprocessor is selected by C86 as shown below.

C86	MPU type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 TO D7
HIGH	6800-SERIES	$\overline{CS1}$	CS2	A0	E	R/W	D0 TO D7
LOW	8080-SERIES	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 TO D7

A0,/WR(OR R/W)AND /RD(OR E) identify the type of parallel data transfer to be made as shown below

common	6800 series			
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read out
1	0	1	0	Display data write
0	1	0	1	status read
0	0	1	0	write to internal register(command)

Chip select input

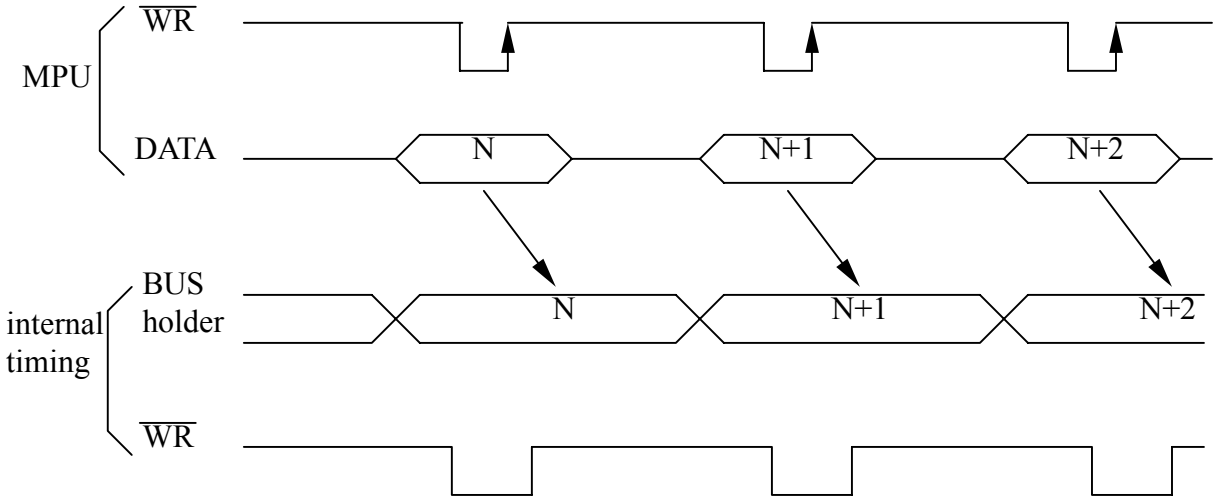
The LCM has two chip select :/CS1 and CS2,and data exchange between the microprocessor and the LCM is enabled when /CS1 is LOW and CS2 is HIGH .When these pins are set to any other combination,D0 toD7 are high impedance .

DATA Transfer

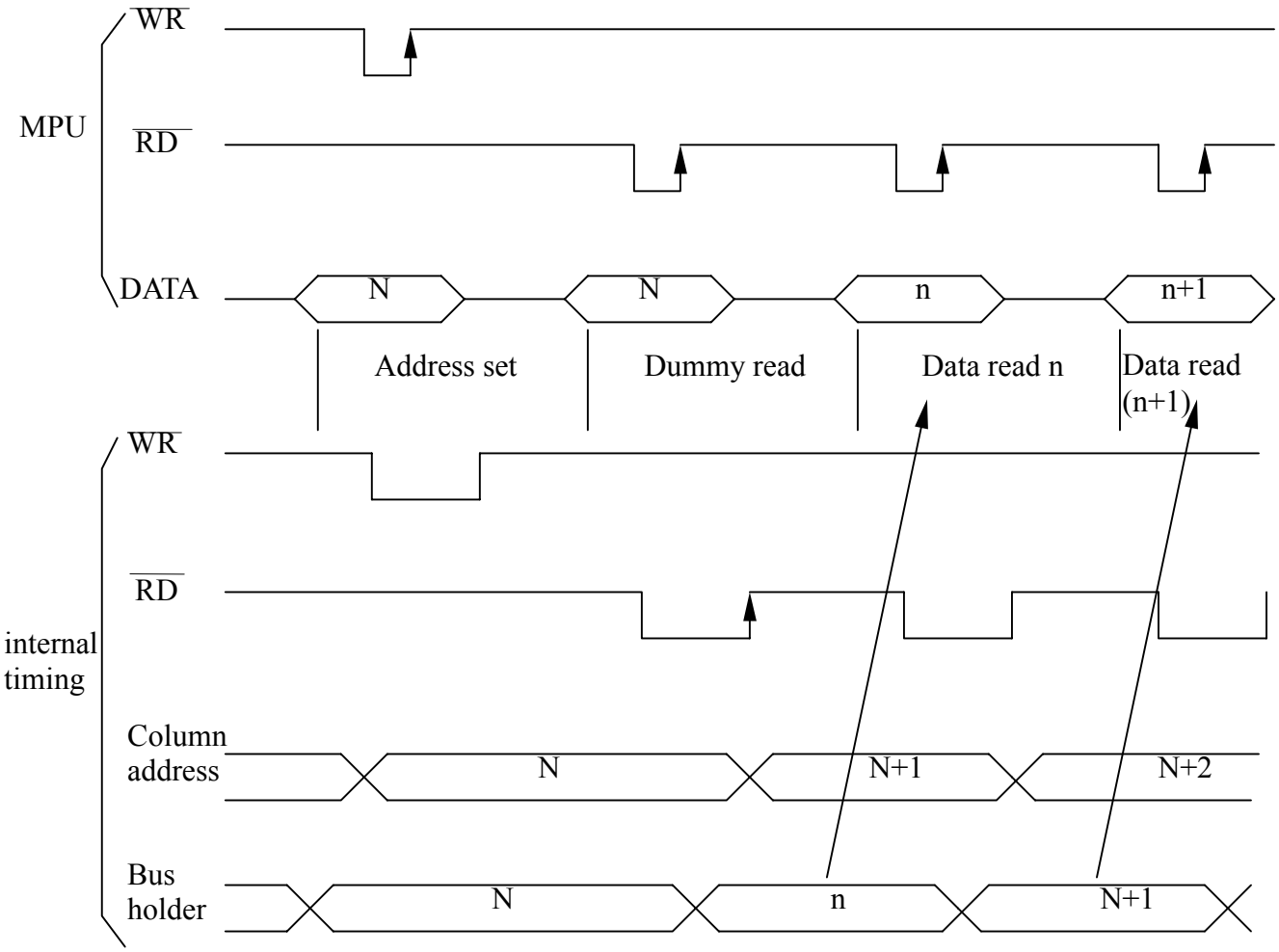
The match the timing of the display data RAM and registers to that of controlling microprocessor, the LCM uses an internal data bus and bus buffer . A kind of pipeline takes place . When the microprocessor reads the contents of RAM , the data for the initial read cycle is first stored in the bus buffer (dummy read cycle) . On the next read cycle , the data is read from the bus buffer onto the microprocessor bus . At the same time , the next block of data is transferred from RAM to the bus buffer . Likewise , when the data is first stored in the bus buffer before being written to RAM at next write cycle .

When writing data from the microprocessor to RAM , there is no delay since data is automatically transferred from the bus buffer to the display data RAM . If the data rate is required to slow down , the microprocessor can insert an NOP instruction which has the same affect as executing a wait procedure .

When a sequence of address sets is executed , a dummy read cycle must be inserted between each pair of address sets . this is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer , before it is sent to the microprocessor . A dummy read cycle is thus necessary after an address set and after a write cycle .



Write timing



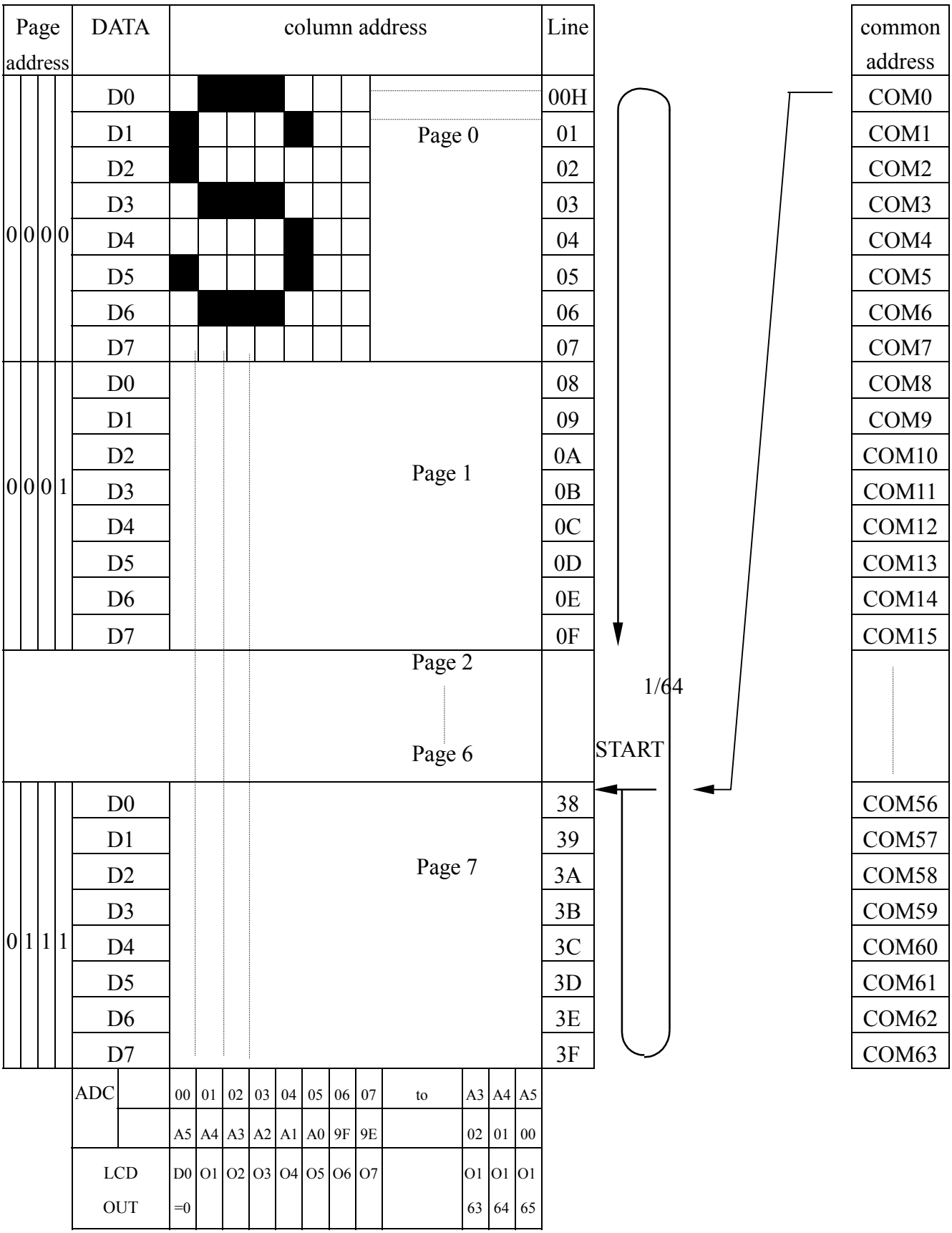
Read timing

Status Flag

The LCM has a single bit status flag ,D7 . When D7 is HIGH , the device is busy and will only accept a Status Read command . If cycle times are monitored , this flag does not have to be checked before each command , and microprocessor capabilities can be fully utilized .

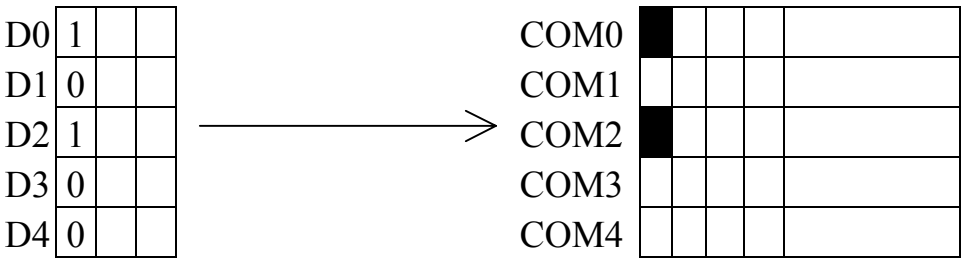
Display Data RAM

The display data RAM stores pixel data for the LCD . It is a 166-column × 65-row addressable array as shown as below



Note

The 65 rows are divided into 8 pages of lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7 . The time taken to transfer data is very short , because the microprocessor inputs D0 toD7 correspond to the LCD common line as show below .



The microprocessor read from and write to RAM through the I/O buffer . Since the LCD controller operates independently , data can be written to RAM at the same time as being displayed , without causing the LCD to flicker .

Column Address Counter

The column address counter is an 8-bit presentable counter that provides the column address to display data RAM . It is incremented by 1 each time a read or write command is received . The counter automatically stops at the highest address counter , A6H . The contents of the column address counter are changed by the Column Address Set command . This counter is independent of the page a address register .

When the select ADC command is used to select inverse display operation , The column address decoder inverts the relationship between the RAM column data and the display segment outputs .

Page Address Register

The 4-bit page address register provides the page address to display data RAM . The contents of the register are changed by the Address Set command .

Page address 8(D3=H , D2 , D1, D0=L) is a special use RAM area for the indicate .

Initial Display Line Register

The initial display line register stores the address of the RAM line that corresponds to the first (normally the top) line (com0) of the display . The contents of this 6-bit register are changed by the initial display line command . At the start of each LCD frame , synchronized with SYNC , the initial line is copied to the line counter . the line counter is then incremented on the CL clock signal once for every display line . this generates the line address for transfer of the 166 bits of RAM data to the LCD drivers . If a 1/65 or 1/33 display duty cycle is selected by the duty+1 command , the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected . If the Duty+1

command is not used , the indicator special-use line address is not selected .

COMMANDS

The Command Set

A0 , /RD(E) and /WR(R/W) identify the data bus commands . Interpretation and execution of commands are synchronized to the internal clock .Since a busy check is normally not needed , commands can be processed at high speed .For the 80-series MPU interface , the command is activated when a low pulse is entered in the /RD pin during read or when a low pulse is entered in the /WR pin during write . While the 68-series MPU interface is set to the read status when the high pules is entered in the R/W pin , and it is set to the write status when a low pules is entered in this pin . The command is activated when a high pules is entered in the E pin . Therefore , the 68-series MPU interface differs from the 80-series MPU interface in the point where the /RD(or E) signal is 1(or high) during status read and during display data read explained in the command description and on the command table . The following command description uses an 80-series MPU interface example . If the series interface is selected , data is sequentially entered from D7 .

COMMAND	**Code**											**Function**
	A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LC display ON and OFF 0:OFF 1::ON
Display START Line set	0	1	0	0	1	Display start address						Determines the RAM display line for CM0
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register
Column address set; high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high-order 4 bits of the display RAM column address in the register .
Column address set; low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RAM column address in the register
Status read	0	1	0	Status				0	0	0	0	Read the status informant
Display data write	1	1	0	Write Data								Write data in the RAM
Display data read	1	0	1	Read Data								Read data in the RAM

COMMAND	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
ADC select	0	1	0	1	0	1	0	0	0	0	1 0	Outputs the display RAM address for SEG. 0:Nornal 1:Reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Displays the LCD image in normal or reverse mode . 0:Nornal 1:Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	lights all indicators 0:Normal display 1:All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0:1/24,48, 1:1/32,64
Duty+1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0:Nornal 1:Duty+1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the line reverse driving and No. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving
Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address count, and set to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0	0: Power OFF 1: Power ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indictors.

Display ON/OFF

Alternatively turns the display ON and OFF.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

Note

D=0 Display OFF

D=1 Display ON

Initial Display Line

Loads the RAM line address of the initial display line , COM0 , into the initial display line register .The RAM display data becomes the top line of the LCD screen . It is followed by the lighter number lines in ascending order . corresponding to the duty cycle . The screen can be scrolled using this command by incrementing the line address .

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			↓			↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Page Address Set

Loads the RAM page address from the microprocessor into the page address register . A page address , along with a column address , defines a RAM location for writing or reading display data . When the page address is changed , the display status is not affected . Page address 8 is a special use RAM area for the indicator . Only D0 is available for data exchange .

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	A5	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

Column Address Set

Loads the RAM column address from the microprocessor into the column address register . The column address is divided into two parts-4 high-order bits and low-order bits. When the microprocessor reads or writes display data to or from RAM , column address are automatically incremented , Starting with the address stored in the column address register and ending with address 166 .

A0	E $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	A7	A6	A5	A4

A0	E $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			↓					↓
1	0	1	0	0	1	0	1	165

Read status

Indicates to the microprocessor the four SED1560 status conditions .

A0	E $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	ON/ OFF	RES- ET	0	0	0	0

BUSY

Indicates whether or not the SED1560 will accept a command . If BUSY is 1 , the device is currently executing a command or is resetting , and no new commands can be accepted . If BUSY is 0 , a new command can be accepted . It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed .

ADC

Indicates the relationship between RAM column address and the segment drivers . If ADC is 1 , the relationship is normal and column address n corresponds to segment driver n. If ADC is 0 , the relationship is inverted and column address(165-n) corresponds to segment driver n .

ON/OFF

Indicates whether the display is ON or Off . If ON/OFF is 1 , the display is OFF . If ON/OFF is 0 , the display is ON . Note that this is the opposite of the Display ON/OFF command .

RESET

Indicates when initialization is process as the result of RES or the Reset command.

Write Display Data

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers . The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page .

A0	E $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Read Display Data

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers . The column address is incremented automatically so that the microprocessor can continously . read data from the addressed page . A dummy read is required after loading an address into the column address register . Display data cannot be read through the serial interface .

A0	E $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Select ADC

Selects the relationship between the RAM column addresses and the segment drivers . When reading or writing display data , the column address is incremented as show in figure4.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	1	0	0	0	0	D

Note

D=0 Rotate right (normal direction)

D=1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor . There are very few restriction on pin assignments when constructing an LCD module .

Normal/Inverse Display

Determines whether the data in RAM is displayed normally or reversed .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	1	0	0	1	1	D

Note

D=0 LCD segment is ON when RAM data is 1(normal) .

D=1 LCD segment is ON When RAM data is 0(inverse).

Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM . The RAM . contents are not changed . This command has priority over the normal/inverse display command .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

Note

D=0 Normal display status

D=1 All display segments ON

If this command is received when the display status is OFF , the Power Save command is executed .

Select Duty

Selects the LCD driver duty . Since this independent from contents of the output status register , the duty must be selected according to the LCD output status .

In multi-chip configuration . the master and slave devices must have the same duty .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

Model	D	Duty
SED1561	0	1/24
	1	1/32

Duty+1

Increase the duty by 1. If 1/48 or 1/64 duty is selected in the SED1560 for example , 1/49 or 1/65 is set , respectively and COM1 functions as either the COM48 or COM64 output . The display line always accesses the RAM area corresponding page address 8 , D0 .(Refer to Figure 4.) In multi-chip configuration , the Duty+1 command must be executed to both the master sides .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

D	Duty
0	1/24 or 1/32
1	1/25 or 1/33

Set n-line Inversion

Selects the number of inverse lines for the LCD AC controller . The value of n is set between 2 to 16 and is stored in the n-line inversion register .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	00	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of inverted line
0	0	0	0	-
0	0	0	1	2
0	0	1	0	3
		↓		↓
1	1	1	0	15
1	1	1	1	16

Cancel n-line inversion

Cancels n-line inversion n-line inversion and restores the normal 2-frame AC control . The contents of the n-line inversion register are not changed .

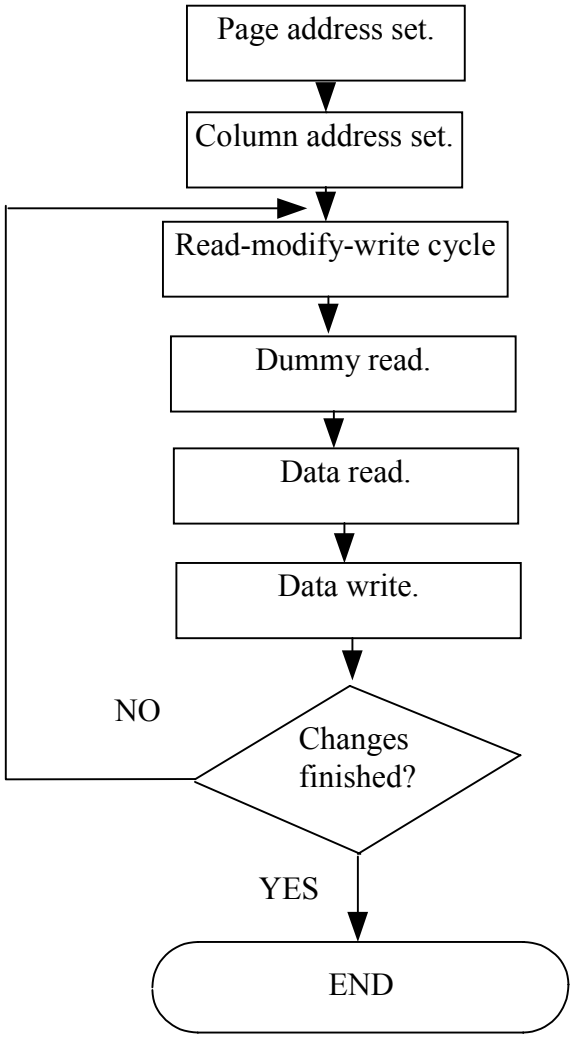
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0

Modify Read

Following this command , the column address is no longer incremented automatically by a Read Display Data command . The column address is still incremented by the Write Display Data command . This mode is cancelled by the End command . The column address is then returned to its value prior to the Modify Read command . This command makes it easy . to manage the duplication of data from a particular display area for feature such as cursor blinking

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note That the Column Address Set command cannot be used in modify-read mode .



END

Cancels the modify read mode . The column address prior to the Modify Read command is restored .

A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

Resets the initial display line , column address , page address , and n-line inversion registers to their initial values . This command dose not affect the display data in RAM .

A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply . Only RES can be used to initialize the supplies .

Output Status Register

A vailable only in the SED1560 and SED1561 . This command selects the role of the COM/SEG dual pins and determines the LCD driver output status. The COM output scanning direction cad be selected by setting A3 to ‘H’ or ’L’ . For details , refer to the Output Status Circuit in each function description.

A0	E/RD	R/W/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

A2	A1	A0	Output Status	Number of COM/SEG Output pins	Remarks
0	0	0	Cause 6	SEG 166	Applies to the SED 1560/61
0	0	1	Cause 5	SEG 134,COM 32	Applies to the SED 1561
0	1	0	Cause 4	SEG 134,COM 32	
0	1	1	Cause 3	SEG 134,COM 32	
1	0	0	Cause 2	SEG 102,COM 64	Applies to the SED 1560
1	0	1	Cause 1	SEG 102COM 64	
1	1	0	Cause 6	SEG 166	Applies to the SED 1560/61
1	1	1	Cause 6	SEG 166	

LCD Power Supply ON/OFF

Turns the SED156*D*B internal LCD power supply ON or OFF . When the power supply is ON , The voltage converter , the voltage regulator circuit and the voltage followers are operating . For the converter to function , the oscillator must also be operating .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	D

Note

D=0 Supply OFF D=1 Supply ON

When an external power supply is used with the SED156*D*B , the internal supply must be OFF . If the SED156*D*B is used in a multiple-chip configuration , an external power supply that meets the specification of the LCD panel must be used . An SED1560operating as a slave must have its internal power supply turned OFF .

Completion of Built-in Power On

This command turns on the built-in power supply .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

The SED1560 series has the built-in , low-power LCD driving voltage generator circuit which can almost all currents except those required for LCD display . This is the primary advantage of the SED1560 series product . However , it has the low power and you need perform the following power-on sequence when turning on the built-in power supply ;

Electronic Volume Control Register

Through these commands , the liquid crystal driving voltage V5 being outputted from the voltage regulation circuit of the built-in liquid crystal power supply , in order to adjust the contrast of the liquid crystal display . by setting data to the 4 bit register , one of the 16 voltage status may be selected for the liquid crystal driving voltage V5 . External resistor are used for setting the voltage regulation range of the V5 . For detail refer to the paragraph of the voltage regulation circuit in the Clause for the explanation of functions

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	A5	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	1 V5l
0	0	0	0	0	Small(as the absolute value)
1	1	1	1	1	Small(as the absolute value)

When not using the electronic volume control function , set to (0,0,0,0,0).