ALL ELECTRONICS
CATALOG # LCD-51

EG SERIES

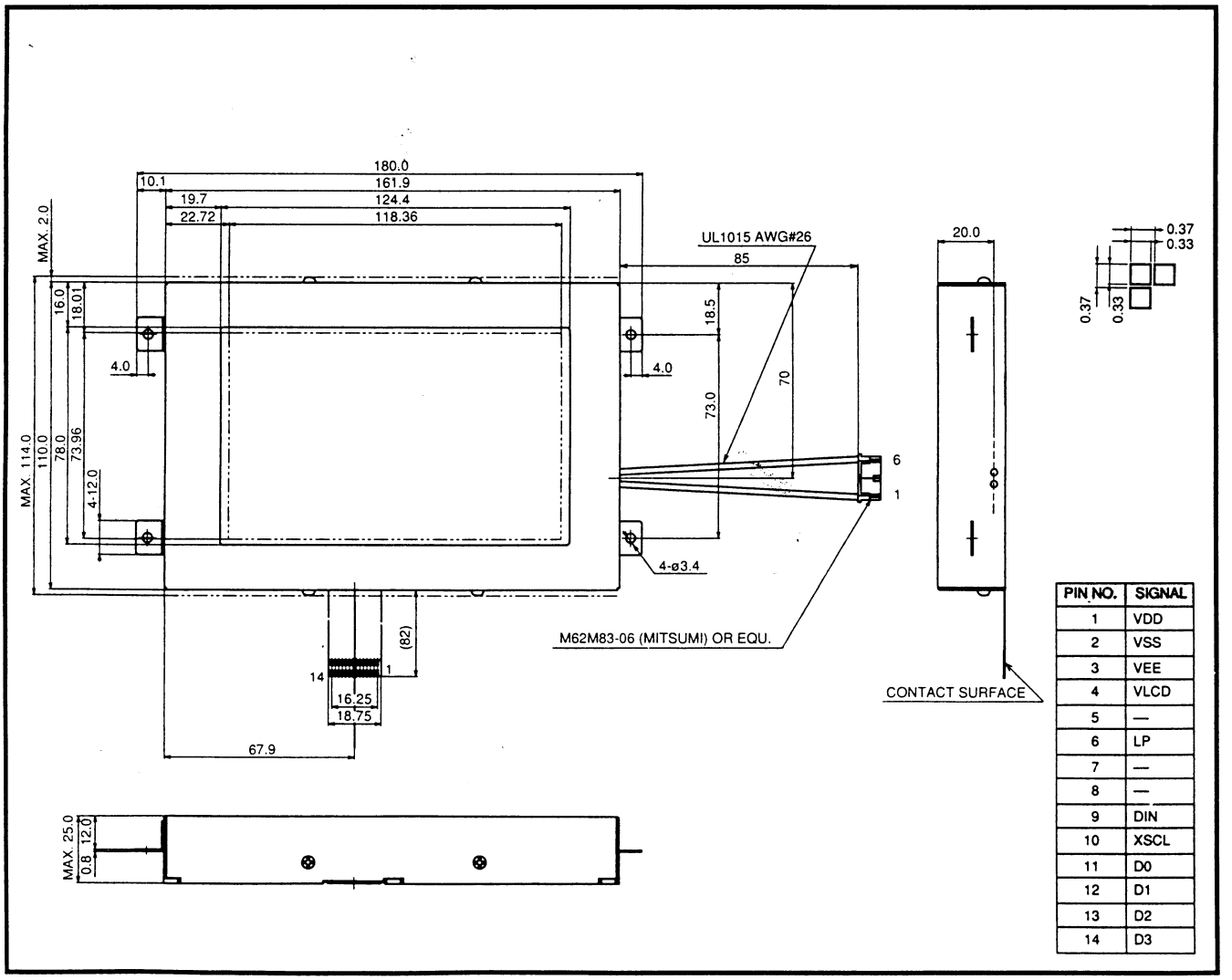
EPSON

EG7501D-LS

- Dot Matrix : 320 x 200 Dots
- Dot Ratio : 1 : 1
- Duty : 1/200
- LCD Mode : FTN, Transmissive Negative Type
- Backlight : CCFT Backlight (One Tube)
- Dot Color : White (Display) Black (Background)
- Mating I/O Connector : 5597-14APB/ 5597-14CPB (Molex)

Parameter	Dimensions (mm)
Overall Size	161.9 x 110.0 x 25.0
Viewing Area	124.4 x 78.0
Active Area	118.36 x 73.96
Dot Pitch	0.37 x 0.37
Dot Size	0.33 x 0.33
Weight	360 (g)

■ Outline Dimensions



PIN NO.	SIGNAL
1	VDD
2	VSS
3	VEE
4	VLCD
5	—
6	LP
7	—
8	—
9	DIN
10	XSCL
11	D0
12	D1
13	D2
14	D3

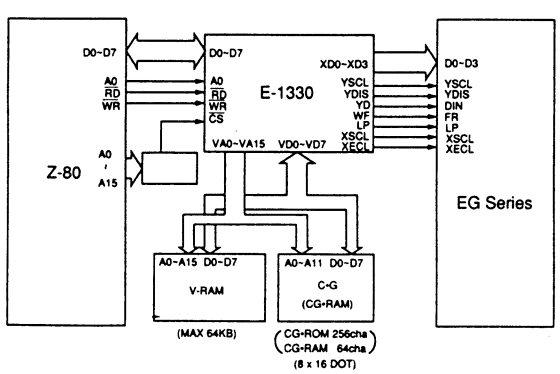
■ Description of Terminals

Symbol	Function	Symbol	Function
VDD	Power supply (+5V)	**DIN**	Synchronous pulse
VSS	Power supply (GND)	**XSCL**	X shift clock
VLCD	Power supply for operating LCD	**XECL**	Enable clock
LP	Latch pulse	**UD0 ~ UD3**	Upper screen display data
FR	Frame pulse	**LD0 ~ LD3**	Lower screen display data
YDIS	Display control, "L"=blank, "H"=normal	**EI**	Lower driver enable input
YSCL	Y shift clock	**EO**	Upper driver enable output

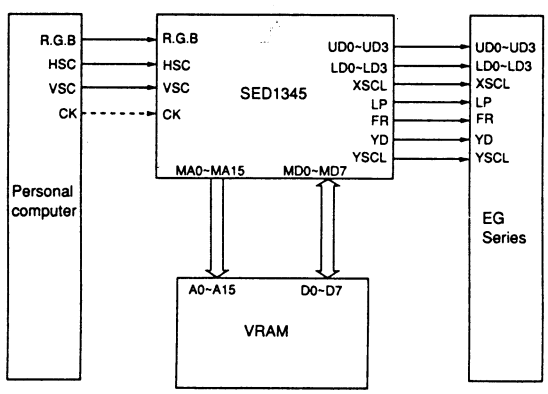
Note: Some signals are not required depending on models.

■ Connecting Block Diagram

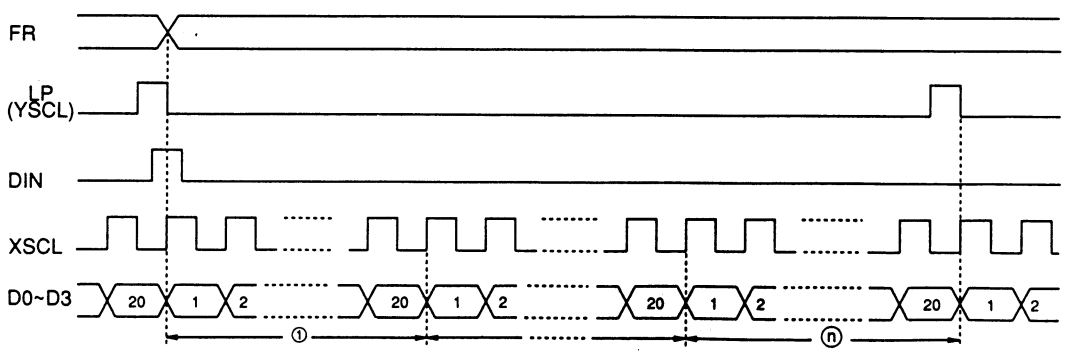
Display in microcomputer control



Display in video signals



■ Timing Chart



(1) to (n) indicate cascade numbers of drivers.

■ Absolute Maximum Ratings

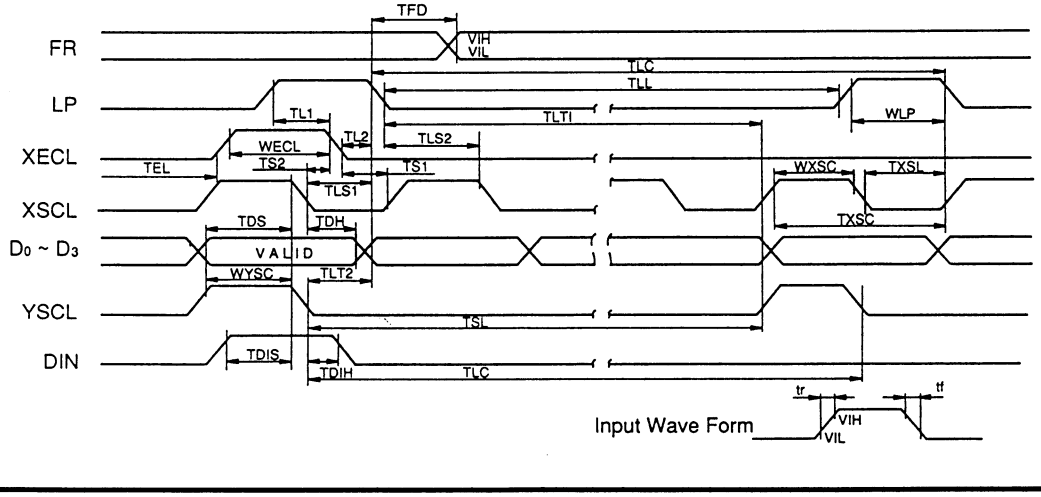
Parameter	Symbol	STD Value	Unit
Supply Voltage	VDD-VSS	0 ~ +7	V
	VDD-VLCD	0 ~ +28.0	V
Input Voltage	VIN	VSS ≦ VIN ≦ VDD	V
Operating Temperature	Top	0~50 (+5 ~ 45: CCFT)	°C
Storage Temperature	Tst	–20~60 (–20 ~ +50: CCFT)	°C

■ AC Characteristics

Ta: 25°C, VDD=5V ±5%

Item	Symbol	Standard Value			Unit
		MIN	TYP	MAX	
FR Delay Time	TFD	–500	0	500	nSec
YSCL. LP Period	TLC	–	Note	–	µSec
XSCL Period	TXSC	166	–	–	nSec
YSCL "L" Time	TSL	180	–	–	nSec
LP "L" Time	TLL	220	–	–	nSec
XECL "L" Time	TEL	100	–	–	nSec
XSCL "L" Time	TXSL	63	–	–	nSec
XECL Set Up Time	TL1	140	–	–	nSec
XECL Hold Time	TL2	50	–	–	nSec
Latch Timing	TLT1	125	–	–	nSec
	TLT2	0	–	–	
	TLS1	100	–	–	
	TLS2	0	–	–	
Latch Pulse Width	WLP	250	–	–	nSec
XSCL Pulse Width	WXSC	63	–	–	nSec
YSCL Pulse Width	WYSC	180	–	–	nSec
XECL Pulse Width	WECL	100	–	–	nSec
XECL Switching Time "H"	TS1	70	–	–	nSec
XECL Switching Time "L"	TS2	–10	–	–	nSec
Data Set Up Time	TDS	50	–	–	nSec
Data Hold Time	TDH	30	–	–	nSec
DIN Set Up Time	TDIS	100	–	–	nSec
DIN Hold Time	TDIH	30	–	–	nSec
Rise Time	tr	–	–	50	nSec
Fall Time	tf	–	–	50	nSec

■ Timing Chart



■ Precautions on Operation

- Keep the specification value of VIL, VIH (Shortening the signal cable) to avoid electrical noise and disturb.
- Follow the power on/off sequence shown in Fig. 1 to prevent a latch-up or DC operation of the LCD Module.
- No LCD module must exceed the absolute maximum ratings. If a module is operated with any exceeded value, its performance will deteriorate and may not longer be restored to normal state.

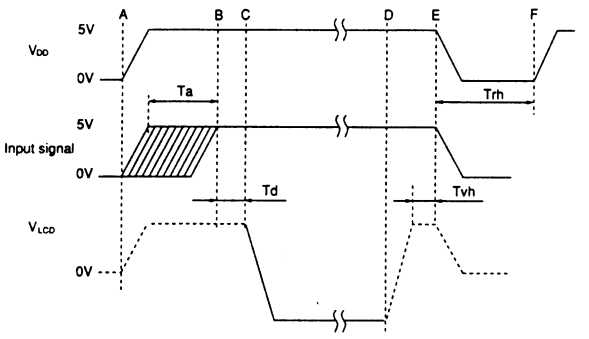


Fig. 1 Power On/Off Sequence

A : +5V Power supply On
B : All signals fixed (Normal operation signal)
C : Minus power supply On
D : Minus power supply Off
E : +5V power supply Off
Frt : +5V power supply re-energizing
Ta : Time of signals not fixed
Td : Delay time of power supply for LCD (Min. 0ms)
Tvh : VDD holding time (Min. 0ms)
Trh : Waiting time for re-energizing (Min. 50ms)

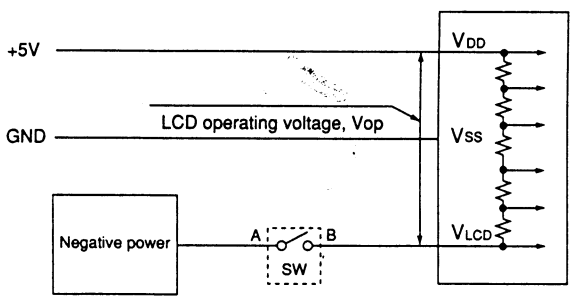


Fig. 2 Typical Example of Power Connection

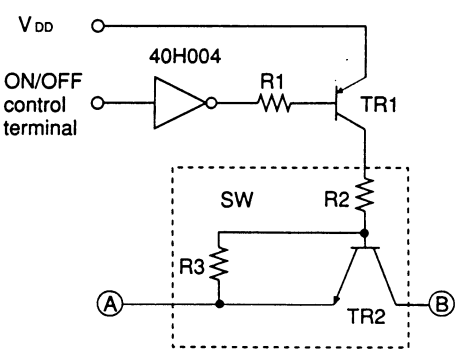


Fig. 3 Typical Example of SW Circuit

Note 1) Fig. 1 shows the voltage levels on module terminals connected with power supply and signal line.
2) VLCD on Fig. 1 shows Off state of switch shown Fig. 2 with a dashed line, On state with a solid line.
3) A circuit example for the SW portion of Fig. 2 is given in Fig. 3.
4) The minus voltage on Fig. 2 should be satisfied at least with the LCD power current shown in the DC characteristics.