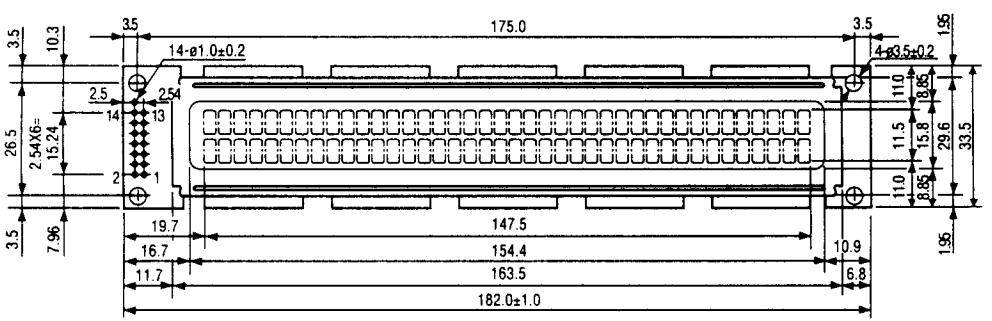
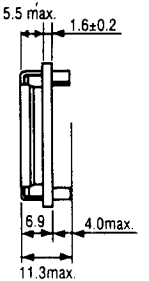
L4042 (2X40) Unit : mm General Tolerance ±0.5 mm

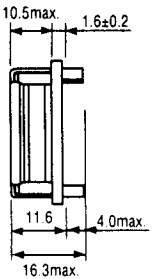
CAT# LCD-70

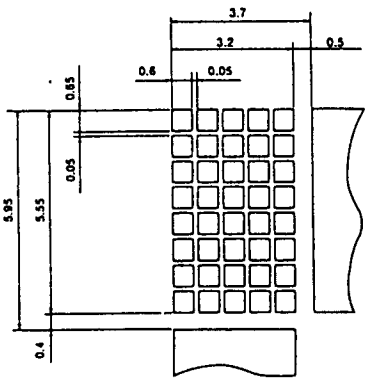


Reflective/EL Backlight



LED Backlight





Pin Functions

No.	Name	Function
1	V_{ss}	GND
2	V_{DD}	Power supply voltage + 5 V
3	V_{LC}	Liquid crystal driving voltage
4	RS	L: Instruction code input. H: Data input
5	R/W	L: Data write from MPU to LCM. H: Data read from LCM to MPU
6	E	Enable
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line

OPERATING INSTRUCTIONS

INTRODUCTION

Seiko Instruments intelligent dot matrix liquid crystal display modules have on-board controller and LSI drivers, which display alpha numerics, Japanese KATA KANA characters and a wide variety of other symbols in either 5 x 7 dot matrix.

The internal operation in the KS0006 controller chip is determined by signals sent from the MPU. The signals include: 1) Register select RS input consisting of instruction register (IR) when RS = 0 and data register (DR) when RS = 1; 2) Read/write (R/W); 3) Data bus (DB7~ DB0); and 4) Enable strobe (E) depending on the MPU or through an external parallel I/O port. Details on instructions data entry, execution times, etc. are explained in the following sections.

READ AND WRITE TIMING DIAGRAMS AND TABLES

The following timing characteristics are applicable for all of Seiko's LCD dot matrix character modules.

READ TIMING CHARACTERISTICS

V_{DD}=5.0V±5%, V_{SS}=0V, T=0°C TO 50°C

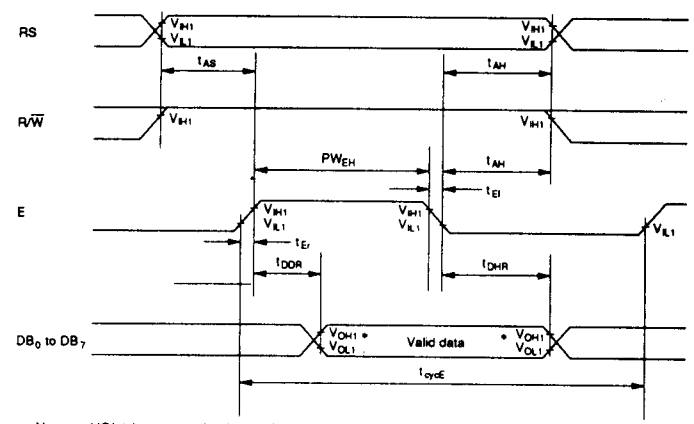
Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W—E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	—	160	ns
Data hold time	t_H	5	—	ns

WRITE TIMING CHARACTERISTICS

V_{DD}=5.0V±5%, V_{SS}=0V, T=0°C TO 50°C

Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W—E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	80	—	ns
Data hold time	t_H	10	—	ns

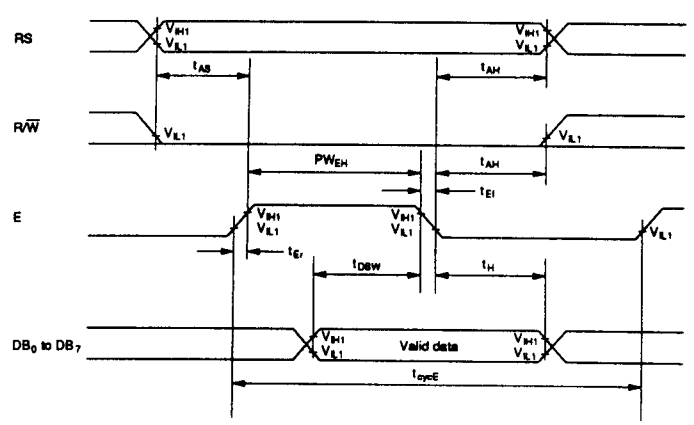
READ OPERATION



Note: * VOL1 is assumed to be 0.8 V at 2 MHz operation.

DATA READ FROM MODULE TO MPU

WRITE OPERATION



DATA WRITE FROM MPU TO MODULE

INSTRUCTION CODES

Instruction	Set		Instruction Code								Description	Execution Time (when f_{cp} or f_{osc} is 250 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μs ~ 1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μs ~ 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or to DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs

* Doesn't matter

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD}: DD RAM address corresponds to cursor address
A_C: Address counter used for both DD RAM and CG RAM address

I/D = 1: Increment
I/D = 0: Decrement

S = 1: Display shift
S = 0: No display shift

D = 1: Display ON
D = 0: Display OFF

C = 1: Cursor ON
C = 0: Cursor OFF

B = 1: Blink ON
B = 0: Blink OFF

S/C = 1: Display shift
S/C = 0: Cursor movement

BF = 1: Internal operation in progress
BF = 0: Instruction can be accepted

R/L = 1: Right shift
R/L = 0: Left shift

DL = 1: 8 bits
DL = 0: 4 bits

N = 1: 2 lines (L1671)

F = 0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{osc} is 270 kHz: 40μs x 250/250 = 37μs

INSTRUCTION CODE EXPLANATIONS

The two registers 1) Instruction Register (IR) and the 2) Data Register (DR) in the KS0066 controller chip are directly controlled by the MPU. Control information is temporarily stored in these registers prior to internal operation start. This allows interface to various types of MPUs which operate at different speeds from that of the KS0066, and allows interface from peripheral control ICs. Internal operations of the KS0066 are determined from the signals sent from the MPU. These signals, including register selection signals (RS), Read/Write (R/W) and data bus signals (DB0 - DB7) are polled instructions.

REGISTER SELECTION

RS	R/W	Operation
0	0	IR selection, IR write. Internal operation: Display clear
0	1	Busy flag (DB7) and address counter (DB0 to DB6) read
1	0	DR selection, DR write. Internal operation: DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation: DD RAM or CG RAM to DR

ADDRESS COUNTER (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB0 to DB6; refer to above "Register Selection Table" when RS = 0 and R/W = 1.

CLEAR DISPLAY

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all display memory and return the cursor to the home position. In other words, the cursor returns to the first character block on the first line on all 1, 2, and 4 line character modules except L4044. If the above is entered on E2 (the second controller for lines 3 and 4), the cursor will return to the first character on the third line.

CURSOR HOME

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	1	*

*Doesn't matter

Returns cursor to home position. First line first character blocks on all 1, 2 and 4 line display; except L4044 refer "clear display": (Address 0; A_{DD} "80"). The contents of DD RAM remain unchanged.

RESTRICTIONS ON EXECUTION OF DISPLAY CLEAR AND CURSOR HOME INSTRUCTIONS

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction).	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. • L4052: f_{osc} = 250 kHz • The other modules: f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction.	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

Entry Mode Set

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one block when writing or reading a character code from DD RAM or CG RAM. The cursor automatically moves to the right when incremented by one or to the left if decremented by one.

S: Shifts the entire display to either the right or left when S = 1 (high). When S = 1 and I/D = 1 the display shifts one position to the left. When S = 1 and I/D = 0 the display shifts one position to the right. This right or left shift occurs after each data write to DD RAM. Display is not shifted when reading from DD RAM. Display is not shifted when S = 0.

Display and Cursor ON/OFF Control

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	1	D	C	B

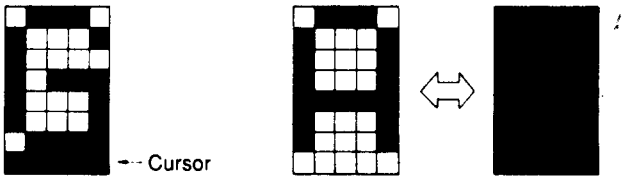
D: Display is turned ON when D = 1 and OFF when D = 0. When display is OFF, display data in DD RAM remains unchanged. Information comes back immediately when D = 1 is entered.

C: Cursor is displayed when C = 1 and not displayed when C = 0. If the cursor disappears, function of I/D etc. does not change during display data write. In a 5 x 7 dot matrix there is an eighth line which functions as the cursor.

B: When B = 1, the character at the cursor position starts blinking. When B = 0 the cursor does not blink. The blink is done by stiching between the all black dot matrix and displayed character at 0.4 second intervals. The cursor and the blink can be set at the same time (fosc = 250 kHz).

5 x 7 DOT MATRIX

C = 1 (cursor display) B = 1 (blinking)



Cursor or Display Shift

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Doesn't Matter

Cursor/Display Shift moves the cursor or shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. In case of a 2-line display, the cursor is shifted from character block 40 of line 1 to character block 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. In case of a 4-line display, the cursor does not move continuously from line 2 to line 3. The cursor is shifted from character block 40 of line 3 to character block 1 of line 4. Displays of lines 3 and 4 are shifted at the same time. The display pattern of line 2 or 4 is not shifted to line 1 or 3.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

FUNCTION SET

	RS	R/W	DB7							DB0
Code	0	0	0	0	1	DL	N	F	*	*

* Doesn't Matter

Function Set sets the interface data length, the number of display lines and the character font.

DL: Interface data length

When DL = 1, the data length is set at 8 bits (DB7 to DB0).

When DL = 0, the data length is set at 4 bits (DB7 to DB4).

The upper 4 bits are transferred first, then the lower 4 bits follow.

N: Number of display lines

F: Sets character font

N	F	Number of display lines	Character font	Duty cycle	
1	0	2	5 x 7 dot matrix	1/16	L1671, L1681, L1672, L1682 L1692, L1634, L2032, L2022 L2034, L2462, L4052, L4044

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

CG RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

CG RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

DD RAM addresses expressed as binary AAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU.

BUSY FLAG/ADDRESS READ

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

The BF signal can be read to verify if the controller is indicating that the module is working on a current instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

DATA WRITE TO CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	0	D	D	D	D	D	D	D	D

← Upper bit Lower bit →

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

DATA READ FROM CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

← Upper bit Lower bit →

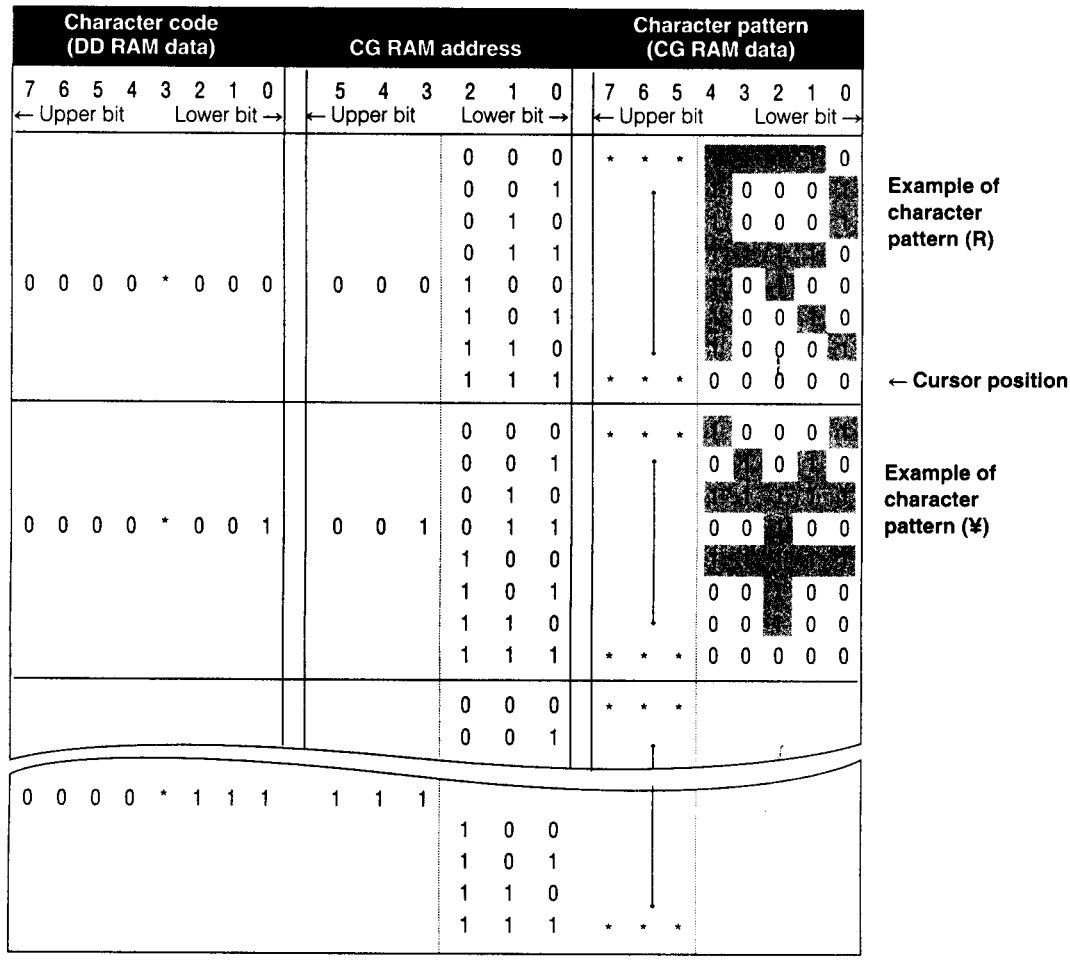
Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. In addition, either instruction is executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note: The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

5 x 7 + CURSOR

Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data), (5 x 7 dot matrix).



NOTES:

- In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.
- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is charged to 1, one bit lights, regardless of the cursor.
- The character pattern column position corresponds to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

PROGRAMMING THE CHARACTER GENERATOR RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to create up to eight custom 5 x 7 characters + cursor (5 x 8). Once programmed, the custom characters or symbols are accessed exactly as if they were in ROM. However since the RAM is a volatile memory, power must be continually maintained. Otherwise, the custom characters/symbols must be programmed into non-volatile external ROM and sent to the display after each display initialization. All dots in the 5 x 8 dot matrix can be programmed, which includes the cursor position.

The modules RAM are divided into two parts: data display RAM (DD RAM) and custom character generator RAM (CG RAM). This is not to be confused programming the custom character generator RAM with the 192 character generator ROM. The CG RAM is located between hex 40 and 7F and is contiguous. Locations 40 thru 47 hold the first custom character (5 x 8), 48 thru 4F hold the second custom character, 50 thru 57 hold the third CG, and so forth to 78 thru 7F for the eighth CG character/symbol.

If during initialization the display was programmed to automatically increment, then only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the completed character is formed. All eight custom CG characters can be programmed in 64 consecutive "writes" after sending the single initial 40 address.

The CG RAM is 8 bits wide, although only the right-most 5-bits are used for a custom CG character row. The left-most dot of programming the CG RAM character corresponds to D4 in the most significant nibble (XXXD4) of the data bus code, with the remaining 4 dots in the row corresponding to the least significant nibble (D3 thru D0), D0 being the right-most dot. Thus, hex 1F equals all dots on and hex 00 equals all dots off. Examples include hex 15 (10101) equal to 3 dots on the hex 0A (01010) equal 2 dots on. In each case the key 5-bits of the 8-bit code program one row of a custom CG character. When all 7 or 8 rows are programmed, the character is complete. A graphic example is shown below:

RS	R/W	Data	Display	Description
0	0	40	—	addresses 1st row, 1st CG character
1	0	11	* *	result of 11, 1st row
1	0	0A	* *	result of 0A, 2nd row
1	0	1F	*****	result of 1F, 3rd row
1	0	04	*	result of 04, 4th row
1	0	1F	*****	result of 1F, 5th row
1	0	04	*	result of 04, 6th row
1	0	04	*	result of 04, 7th row
1	0	00	—	result of 00, 8th row (cursor position)
1	0	15	***	**1st row, 2nd CG character. Note: Addressing not now required; hex 48 is next in the sequence.**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Note: Address locations on lines 1 & 2 are controlled by enabling E1.

CHARACTER FONT CODES (5 x 7 DOT MATRIX)

Upper 4 Bit Hexadecimal

Lower 4 Bit Hexadecimal

Lower 4 bits \ Upper 4 bits	0000 (0)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
××××0000 (0)	CG RAM (1)												
××××0001 (1)	(2)												
××××0010 (2)	(3)												
××××0011 (3)	(4)												
××××0100 (4)	(5)												
××××0101 (5)	(6)												
××××0110 (6)	(7)												
××××0111 (7)	(8)												
××××1000 (8)	(1)												
××××1001 (9)	(2)												
××××1010 (A)	(3)												
××××1011 (B)	(4)												
××××1100 (C)	(5)												
××××1101 (D)	(6)												
××××1110 (E)	(7)												
××××1111 (F)	(8)												

EXAMPLES OF 8-BIT AND 4-BIT DATA TRANSFER OPERATION

DISPLAY INITIALIZATION

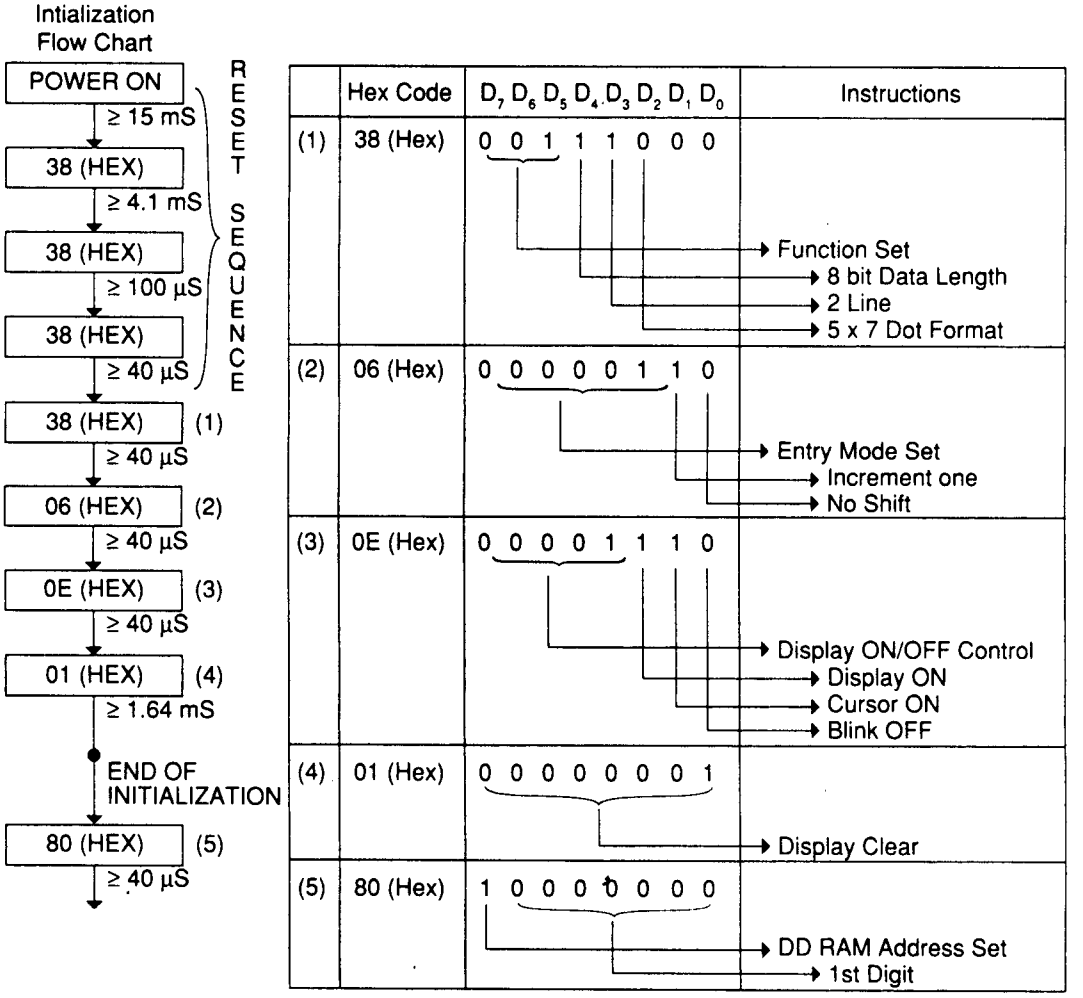
Each time the module is turned on or reset, an initialization procedure must be executed. The procedure consists of sending a sequence of hex codes from the microprocessor or parallel I/O port. The initialization sequence turns on the cursor, clears the display, and sets the module onto an auto-increment mode.

The initial hex code 30, 34, or 38 is sent two or more times to ensure the module enters the 8-bit or 4-bit data mode. All the initialization sequences are performed under the condition of Register Select (RS) = 0 (low) and Read/Write (R/W) = 0 (low).

The 4-bit data bus microcontroller may operate the display module by sending the initialization sequence in 4-bit format. Since 4-bit operation requires the data to be sent twice over the higher 4-bit bus lines (D4-D7), memory requirements are doubled.

A. EXAMPLE FOR THE MODULE WITH 5 x 7 Character Format Under 8-Bit Data Transfer

Applicable modules: L1671, L1681, L1672, L1682, L2032, L2462, L4052, L1634, L2034, L4044



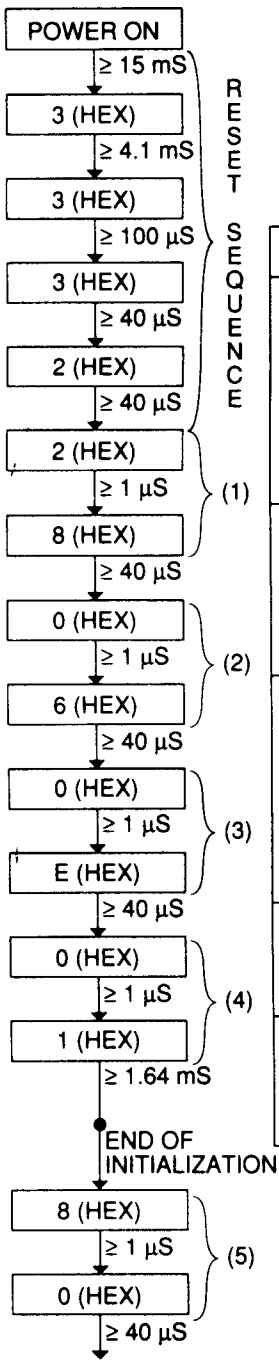
Note:
1) Both RS and R/W terminals shall be "0" in this sequence.
2) RS, R/W and Data are latched at the falling edge of the Enable signal, (falling edge is typically 10nSec; Max: 25nSec).
3) M4024 has to be initialized on E1 and E2 respectively.

EXAMPLES OF 8-BIT AND 4-BIT DATA TRANSFER OPERATION

B. EXAMPLE FOR THE MODULE WITH 5 x 7 Character Format Under 4-Bit Data Transfer

Applicable modules: L1671, L1681, L1672, L1682, L2032, L2462, L4052, L1634, L2034, L4044

Flow Chart



	Hex Code	1st D_7 D_6 D_5 D_4	2nd D_7 D_6 D_5 D_4	Instructions
(1)	2 (Hex)	0 0 1 0		Function Set 4 bit Data Length
	8 (Hex)		1 0 0 0	2 Line 5 x 7 Dot Format
(2)	0 (Hex)	0 0 0 0		
	6 (Hex)		0 1 1 0	Entry Mode Set Increment No Shift
(3)	0 (Hex)	0 0 0 0		
	E (Hex)		1 1 1 0	Display ON/OFF Control Display ON Cursor ON Blink OFF
(4)	0 (Hex)	0 0 0 0		
	1 (Hex)		0 0 0 1	Display Clear
(5)	8 (Hex)	1 0 0 0		
	0 (Hex)		0 0 0 0	DD RAM Address Set 1st Digit

Note: 1) Both RS and R/W terminals shall be "0" in this sequence.
2) RS, R/W and Data are latched at the falling edge of the Enable signal.
3) Enable signal has to be sent after every 4-bit Data transfer.

SAMPLE PROGRAMS

1) Display "THIS IS SEIKO LCD MODULE" on L1672.
   - ▶ Set RS = R/W = 0 (low), then send hex codes 38, 38, 06, 0E, 01, 80. (80 is the home position of the DD RAM)
   - ▶ Set RS = 1 and R/W = 0, then send hex codes 54, 48, 49, 53, 20, 49, 53, 20, 53, 45, 49, 4B, 4F.
   - ▶ Set RS = R/W = 0, then send hex code C0 to start from beginning of the second line.
   - ▶ Set RS = 1 and R/W = 0, then send hex codes 4C, 43, 44, 20, 4D, 44, 55, 4C, 45.

2) Display "ONE", "TWO", "THREE", and "FOUR" on each line of L4044.
   - ▶ Set RS = R/W = E2 = 0, E1 = 1, then send hex codes 38, 38, 06, 0E, 01, 80.
   - ▶ Set RS = R/W = E1 = 0, E2 = 1, then send hex codes 38, 06, 0C, 01.
   - ▶ Set RS = E1 = 1, R/W = E2 = 0, then send hex codes 4F, 4E, 45.
   - ▶ Set RS = R/W = E2 = 0, E1 = 1, then send hex code C0.
   - ▶ Set RS = E1 = 1, R/W = E2 = 0, then send hex codes 54, 57, 4F.
   - ▶ Set RS = R/W = E2 = 0, E1 = 1, then send hex code 0C.
   - ▶ Set RS = R/W = E1 = 0, E2 = 1, then send hex codes 0E, 80.
   - ▶ Set RS = E2 = 1, R/W = E1 = 0, then send hex codes 54, 48, 52, 45, 45.
   - ▶ Set RS = R/W = E1 = 0, E2 = 1, then send hex code C0.
   - ▶ Set RS = E2 = 1, R/W = E1 = 0, then send hex codes 46, 4F, 55, 52.

3) Display "L1671 LCD MODULE" on L1671. (Special case in the LCD modules)
   - ▶ Set RS = R/W = 0, then send hex codes 38, 38, 06, 0E, 01, 80.
   - ▶ Set RS = 1 and R/W = 0, then send hex codes 4D, 31, 36, 34, 31, 20, 4C, 43.
   - ▶ Set RS = R/W = 0, then send hex code C0 to start from 9th character.
   - ▶ Set RS = 1 and R/W = 0, then send hex codes 44, 20, 4D, 4F, 44, 55, 4C, 45.

INTERFACE PROBLEMS AND POSSIBLE SOLUTIONS

Although the following problems and possible solutions are not all inclusive, they do represent the most common problems experienced not only by the first-time user, but also experienced users. If the user is experiencing problems, please review all of the following information. If the user still has problems, please call **Seiko Instruments** in Torrance, California at (310) 517-7770.

SYMPTOMS

1) Display is blank after power ON and initialization: Check 1- 6.
2) Wrong information being displayed: Check 3,4,6,7,8,9.
3) Symptoms same as 2, except multiple components are tied to the data bus: Check 8,9,10.
4) ICs become HOT: Check 1,11,12,13.
5) Cannot enter information to the 2nd line or lines 3 and 4 of the 4-line display: Check 4,14,15.

POSSIBLE SOLUTION(S)

1) Check +5 VDC and ground lines and connections.
2) A variable resistor or fixed resistor must be used on the V_{LC} pin for all LCD modules. V_{LC} voltage range is: 0~.7 volts (ref: Contrast Adjustment Circuit).
3) Data is being transmitted too fast:
   - ▶ Wait 4.5 mS after Power ON, or until V_{DD} reaches 4.5 volts. Wait more than 15 mS after V_{DD} reaches 4.5 volts.
   - ▶ Allow 1.6mS, after entering hexadecimal 01 or 02 at the end of the initialization sequence, then enter data.
   - ▶ Time interval between other data entries should be 50uS or greater.
4) Failure to properly initialize the display: Check initialization examples for either 4 or 8-bit. Make sure to enter first hexadecimal entry at least twice in the initializa tion sequence. This sets the LCD to either a 1 or 2 line display.
5) LCD input assumed to be configured as an IC. (This is not correct.)
6) Check the time interval on the falling edge of the enable pulse. Should not exceed 25nS (typical is 10nS).
7) Enable pulse width is shorter than 450nS.
8) More than one external bus being selected: Check data bus connection.
9) Signal levels are too low: Insure that V(1H) is more than 2.4 volts.
10) All data bus components do not have TTL type outputs.
11) V_{DD} and V_{ss} pins are reversed.
12) Too much voltage on V_{DD} - (Max. 7VDC).
13) Load being put on data lines, when power is OFF on the V_{DD} pin.
14) Check address locations for the first position on the second line for each 2 lines (ref: Address Location Chart).
15) L4044 has two controllers: E1 for lines 1 & 2 and E2 for lines 3 & 4. Initialization must be done for E1 and the same for E2.